APPLICATION NOTE

Unintentional Island Testing

Charting new waters with SL1200 Series grid emulators

KEYSIGHT

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Changing Landscape on Electrical Grids

For over a century, the energy production in electric utility grids has been centralized around a relatively small number of large power-generating stations. Grid regulation and safety have relied on the fact that the utilities have centralized control over the production and flow of energy, as well as the ability to shut down or isolate segments of infrastructure in the event of repairs or maintenance. However, with the ever-increasing integration of renewable energy resources into the power grid, such as solar photovoltaic, battery storage, and wind turbine systems, this centralized mode of control will no longer apply. Because the energy production will incorporate many smaller, distributed sources which are privately owned, numerous standards and rules must be put in place which every one of these energy sources must follow to ensure a safe and stable grid.

Navigating the Treacherous RLCs

Unintentional Islands

One fundamental requirement for grid-tied distributed energy resources (DER) is that they must cease to export power into the grid if utility power is lost. Segments of a circuit may be intentionally disconnected from the grid by the utility for maintenance and repairs or become accidentally separated by broken wires or fuses, leaving an isolated segment with a combination of DERs and loads. Failure of DERs to de-energize an unintentionally isolated segment, resulting in an 'unintentional island', would pose many problems. An unintentional island has unreliable electrical characteristics, can damage equipment, is hazardous to maintenance workers and bystanders, and prevents repairs until the source(s) is located and de- energized. **Figure 1** illustrates the concept of a DER inverter energizing local loads.

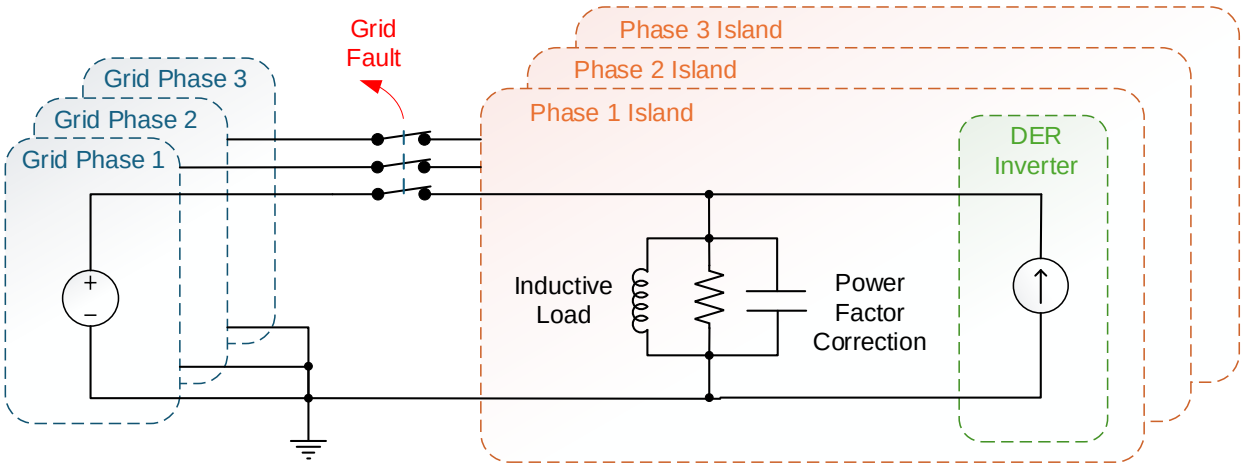

Figure 1. Islanded inverter powers local loads

Without a connection to the main grid, DERs usually cannot continuously energize local loads. When a segment becomes isolated, in most cases, there will be a large mismatch between the power supplied by the DER and the power consumed by loads present on the isolated segment. This imbalance causes sudden, large transients in voltage and line frequency, which fall outside normal operating conditions of the DER inverter, and trip fault protection.

Furthermore, grid-tied DER inverters are not designed to supply a constant voltage like a portable generator. Instead, they modulate their exported power by changing their output current. In other words, they aren't designed to act as stand-alone sources; they are merely energy supplements to the existing grid. **Figure 2** illustrates the unregulated voltage that would occur without connection to the main grid.

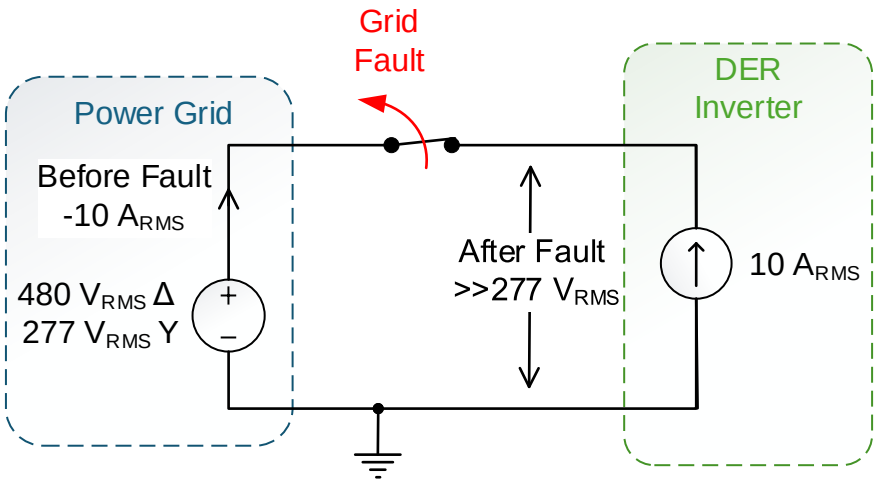

Figure 2. Open circuit fault separates grid and loads from DER. Current source inverter cannot push current into an open circuit, so output voltage increases until overvoltage protection trips and the inverter shuts down.

Nevertheless, under the right loading conditions, it is possible for a grid-tied inverter to be 'fooled' and continue to power local loads on an isolated segment, thus creating a sustained unintentional island. The following conditions are required to create an island with stable voltage and frequency:

1. Matching of real and reactive power generated by the DER and real and reactive power absorbed by the loads.
2. Presence of reactive loading, either inductive, capacitive, or both, which is similar in magnitude to the resistive loading. This creates a resonant RLC tank with a negative phase versus frequency characteristic that stabilizes the island frequency.
3. Occurrence of a high impedance fault which disconnects the segment from the main grid to form the island.

Island Voltage

Island voltage is determined by the instantaneous DER output current and the load impedance. In a simple case of a unity power factor inverter with current '$I_{INVERTER}$' and a resistive load 'R_{ISLAND}':

$$V_{ISLAND} = I_{INVERTER} * R_{ISLAND}$$

Equation 1. Ohm's law of island voltage

By virtue of Ohm's law, meeting the balancing requirements of #1 ensures that $V_{ISLAND} \sim V_{GRID}$. **Figure 3** illustrates this concept. Any mismatch in the balancing of real power prior to the island formation will result in an increase or reduction of the island voltage with respect to nominal. The increase or reduction is a result of conservation of energy within the island: the real power absorbed by the resistive loads matches the real power generated by the DER.

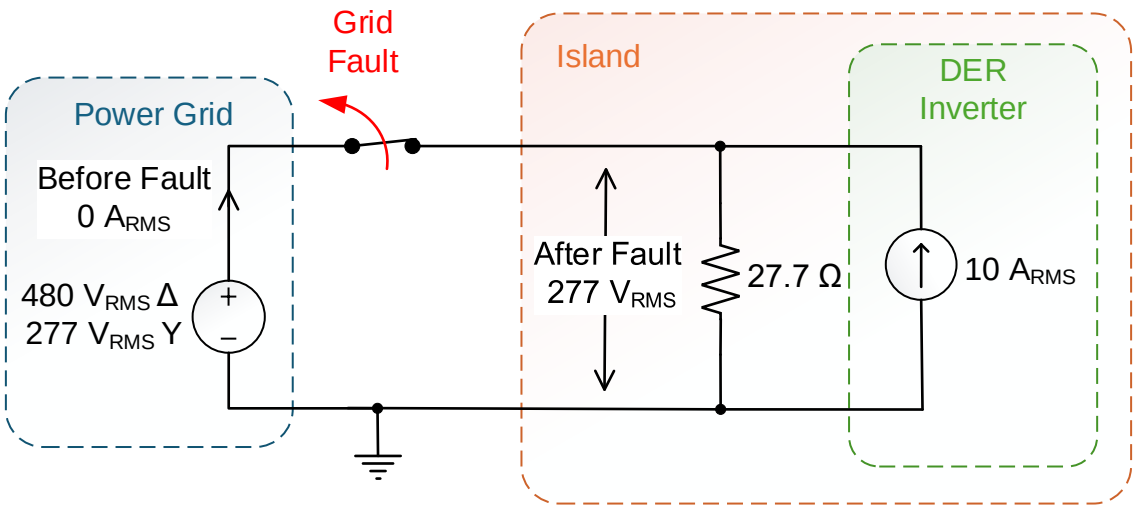

Figure 3. Illustration of island formed with matched R, yielding island voltage equal to the grid voltage

Notably, an island does not have to perfectly match the nominal grid voltage to persist. Variations of ± 10% around nominal grid voltage are considered normal. DERs must continuously operate under these conditions, and under/overvoltage protection must not trip unless these limits are exceeded. Minor voltage deviations from island loading are indistinguishable from normal grid fluctuations. This range of acceptable voltage allows formation of an unintentional island even if the balancing conditions of #1 are imperfect, as illustrated in **Figure 4**.

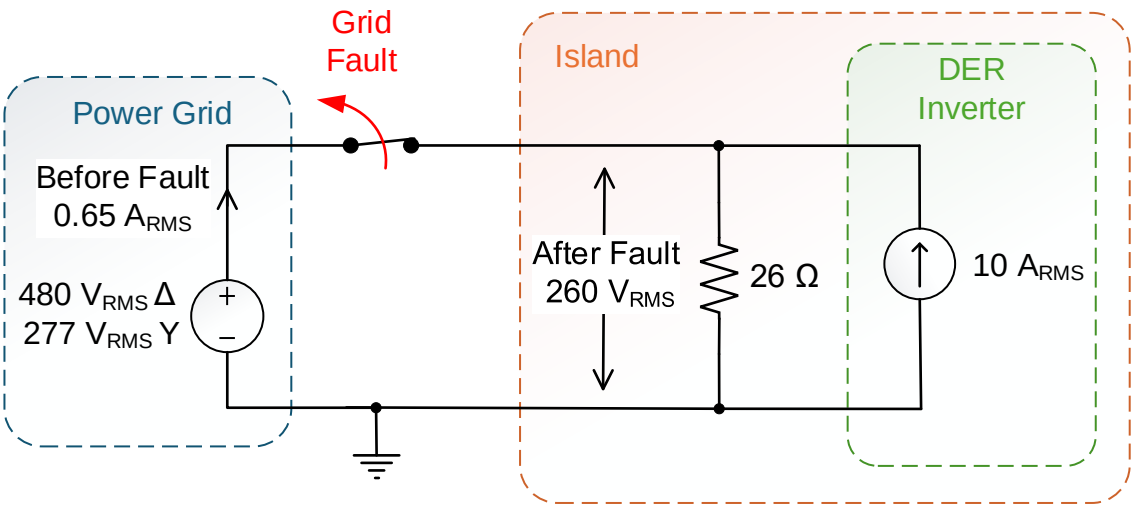

Figure 4. Illustration of island formed with slightly mismatched R, yielding island voltage lower than nominal but within tolerance of required inverter operation.

Island Frequency

Grid-tied inverter protections tend to be more sensitive to frequency than voltage deviations, as the range of tolerable operating frequency is much smaller than the range of anticipated voltage fluctuations. Frequency of an island is governed by the interaction between the DER inverter's internal phase-locked loop (PLL) and the island impedance phase versus frequency characteristic. An example of island frequency stabilization is described in the steps below:

Step 1. Pre-Island

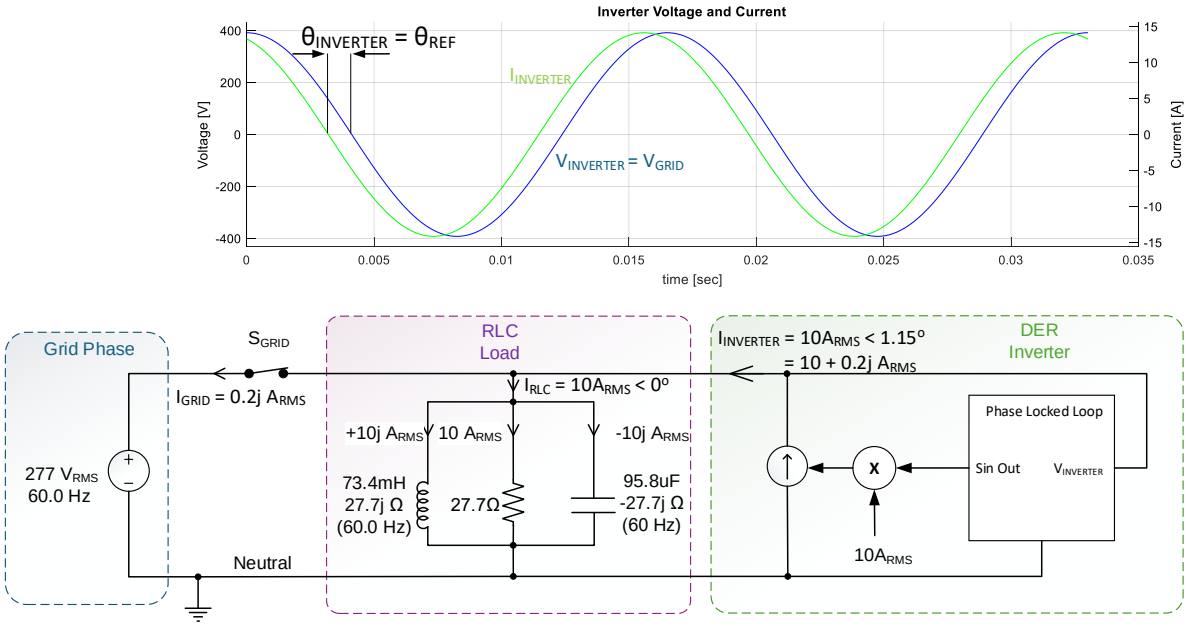

Figure 5. Pre-island conditions before S_{GRID} opens

Under normal operation the inverter PLL tracks a fixed reference sinusoidal voltage, $V_{INVERTER} = V_{GRID}$, and generates a phase-locked sinusoidal current with phase $\theta_{INVERTER} = \theta_{REF}$. In this example, θ_{REF}=1.15° and θ_{RLC} = 0° such that I_{GRID} current is approximately 2% of full scale (0.2A) and purely reactive. θ_{RLC} and θ_{REF} ($\theta_{INVERTER}$) are related to I_{GRID} by Equation 2.

$$\theta_{INVERTER} - (-\theta_{RLC}) \approx arctan\left(\frac{|I_{GRID}|}{|I_{INVERTER}|}\right) = arctan(.02) = 1.15^{o}$$

Equation 2. Relationship between I_{RLC}-to-$I_{INVERTER}$ phase angle discrepancy and I_{GRID}. This assumes I_{RLC} and $I_{INVERTER}$ are similar in magnitude.

This somewhat arbitrary value of θ_{REF} represents realistic nonidealities in inverter phase tracking and still yields a power factor > 0.999, as shown in Equation 3.

$$PF = \cos(\theta_{REF}) = \cos(1.15^{o}) = 0.9998$$

Equation 3. Power factor computed from phase angle

Step 2. S_{GRID} Opens – $V_{INVERTER}$ jumps from -θ_{REF} to θ_{RLC}

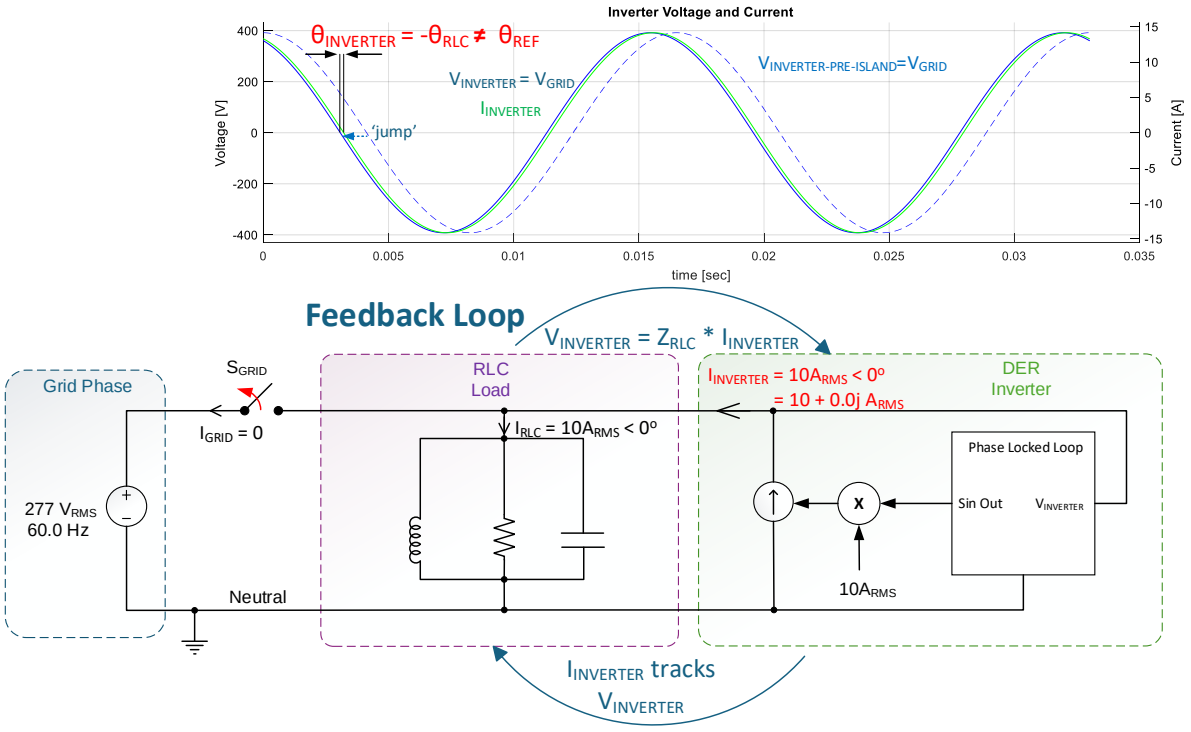

Figure 6. Conditions immediately after S_{GRID} opens

After S_{GRID} opens, $V_{INVERTER}$ is no longer connected to the grid and becomes governed by $Z_{RLC} * I_{INVERTER}$, forming a feedback loop between $V_{INVERTER}$ and $I_{INVERTER}$. Because of the fast response of the RLC tank dynamics, the phase of $V_{INVERTER}$ 'jumps' to θ_{RLC} (with respect to $I_{INVERTER}$) more quickly than the PLL can regulate $I_{INVERTER}$ with respect to $V_{INVERTER}$. The PLL detects a phase error and is temporarily out of phase lock. This initial phase error is given in Equation 4.

$$\Delta\theta = -(\theta_{RLC} + \theta_{REF})$$

Equation 4. Error theta between PLL angle and RLC angle

The PLL begins to 'walk' the frequency in an attempt to correct this phase error. In this example, $\theta_{RLC} = 0^o$, so the initial phase error is -1.15°.

Step 3. Frequency walk to correct $\Delta\theta$

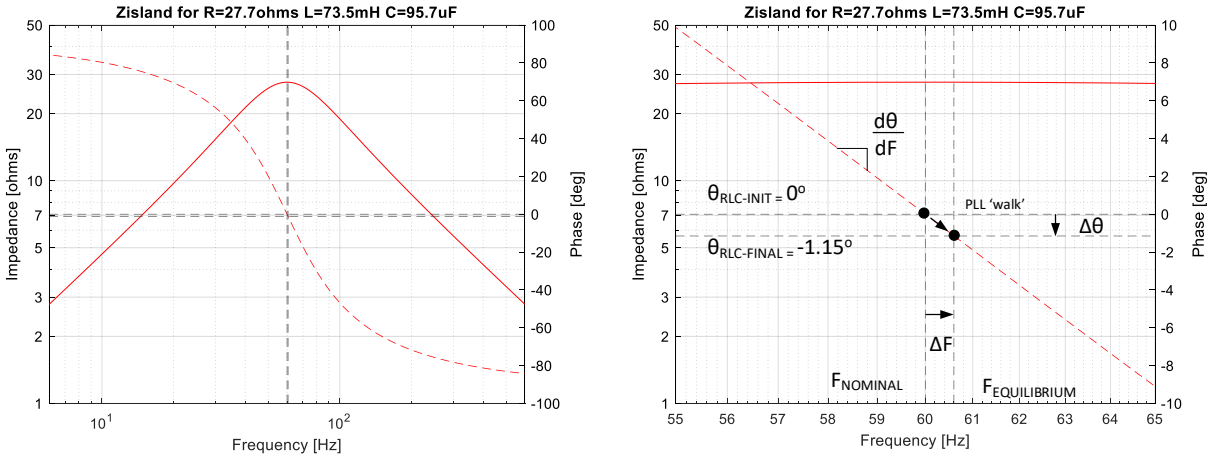

Figure 7. Bode plot of RLC tank impedance (left) and the same plot zoomed in on frequency (right)

The parallel RLC load has a negative phase vs frequency characteristic $\left(\frac{d\theta_{RLC}}{dF}\right)$. As the PLL frequency walks up, the RLC tank impedance, θ_{RLC}, decreases which causes $V_{INVERTER}$ to begin to lag again with respect to $I_{INVERTER}$ and the PLL phase error diminishes. Equilibrium occurs when $\theta_{RLC} = -\theta_{REF}$. This corresponds to a round-trip phase of zero in the island feedback loop. Final frequency deviation from nominal is approximated by

Equation **5**.

$$\Delta F \approx \frac{\Delta\theta}{\left(\frac{d\theta_{RLC}}{dF}\right)} = \frac{1.15^o}{1.9} = 0.6\text{Hz}$$

where $\left|\frac{d\theta_{RLC}}{dF}\right| \approx 1.9$ for an RLC tank with $Q_{FACTOR} = 1$

Equation 5. Linear approximation of RLC phase change with respect to frequency

Note that this assumes θ_{REF} remains unchanged with respect to voltage and frequency, which is not always the case.

Step 4. Post-island equilibrium frequency = 60.6Hz

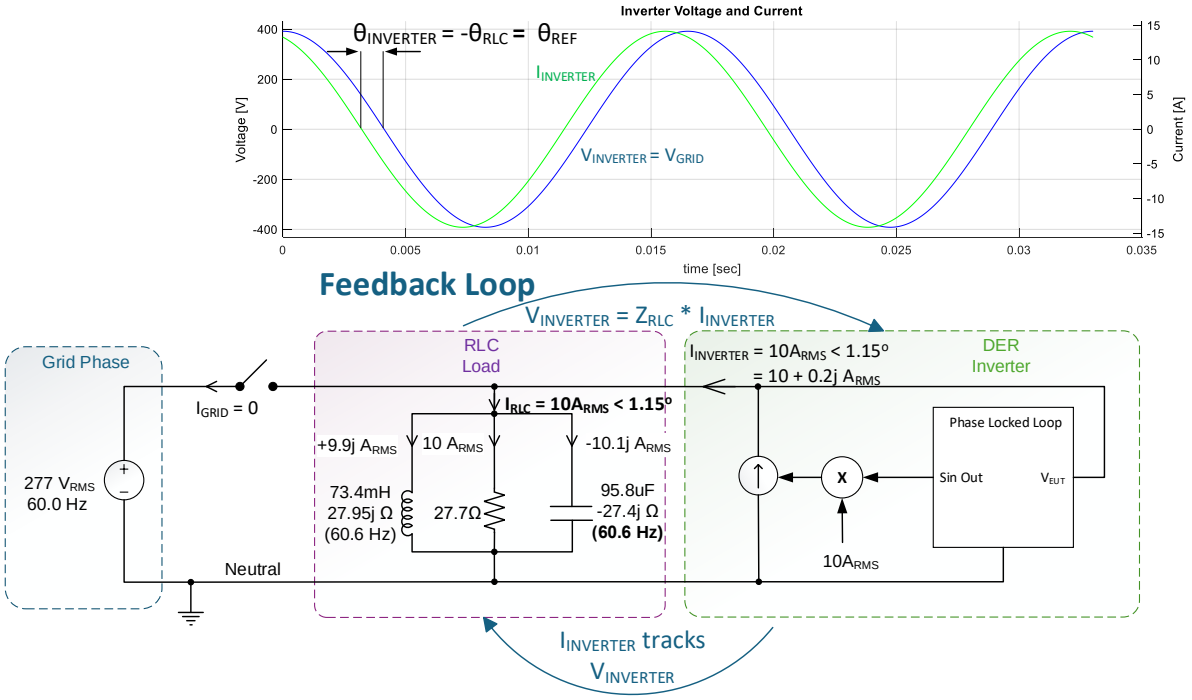

Figure 8. Inverter in equilibrium island state.

The unintentional island can sustain this new equilibrium state indefinitely, as long as the inverter output and RLC impedance are uninterrupted.

One implication in this process is that a lower quality factor (Q_F) RLC tank yields a larger drift in island frequency because the magnitude of $\frac{d\theta_{RLC}}{dF}$ is smaller. See **Equation 6**, **Equation 7**, and **Figure 9**. At the extreme end, a pure resistive load ($Q_F = 0$) with no reactive elements will not form a stable island at all because $\frac{d\theta_R}{dF} = 0$. In this case, after S_{GRID} opens, the PLL will continue to walk the frequency and never be able to correct the phase error.

$$Z_{ISLAND} = R \,||\, j\,2\pi * F * L \,||\, \frac{1}{j\,2\pi * F * C}$$

Equation 6. Impedance of parallel RLC circuit

$$Q_{FACTOR} = \frac{R}{\sqrt{\frac{L}{C}}}$$

Equation 7. Quality factor of parallel RLC circuit

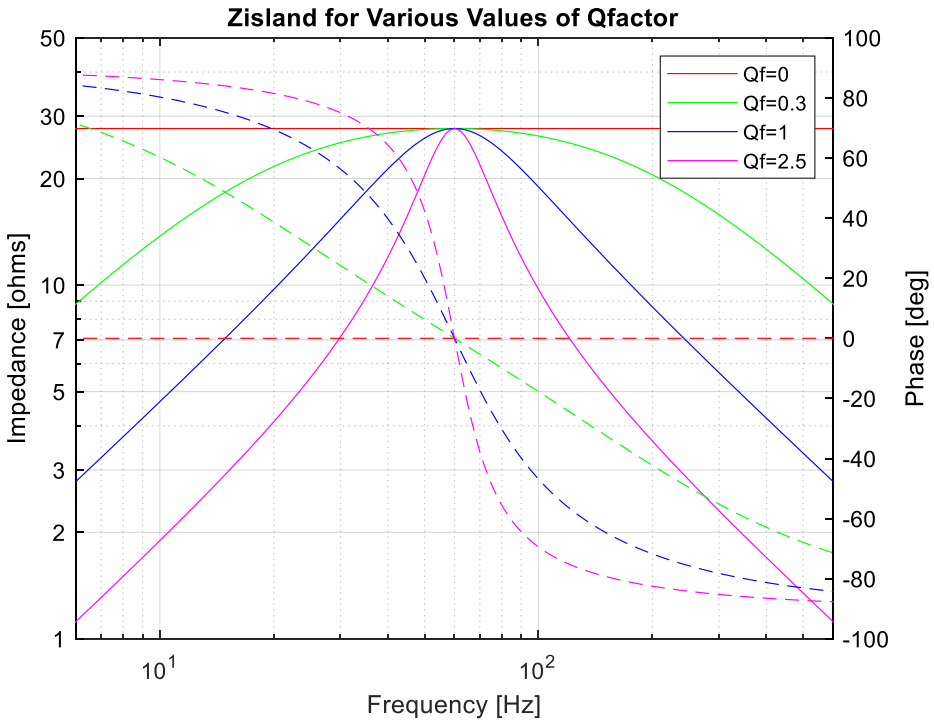

Figure 9. RLC tank impedance magnitude and phase for various values of quality factor. Impedance (solid) and Phase (dashed)

Presence of passive reactive loads on the grid allow the island frequency to stabilize very close to the grid frequency and prevent detection of the island by means of passive frequency monitoring. Prominent loads such as motors and transformers (both industrial and residential scale) have inductive characteristics, and power factor correction capacitors are often installed on the grid to correct for such inductive loads to minimize losses and avoid utility penalty charges.

Anti-Islanding Algorithms

In theory, conditions can be just right to form an island where the stabilized island voltage and frequency are arbitrarily close to nominal levels. Therefore, passive monitoring for abnormal voltage or frequency is not a robust means to detect the loss of grid connection in a grid-tied inverter. Inverters must employ special anti-islanding algorithms that actively disrupt the island enough to detect the condition and shut down. These algorithms are nontrivial to develop, can take on a wide variety of forms, and are usually proprietary technology for each inverter manufacturer. These algorithms tend to fall into several broad categories, each of which has advantages and disadvantages. A paper surveying several anti-islanding methods is found in (Bower & Ropp, 2002). Three examples are described below.

Positive Feedback of Frequency

A commonly employed category of anti-islanding strategy is to deliberately create a positive feedback loop in the frequency of the island. This creates a frequency divergence that is quickly detected by over / under frequency protections. Several methods in this category exist, including the Slip Mode Frequency Shift (Bower & Ropp, 2002) and the Sandia Frequency Shift (Menghua Liu, 2021), which accomplish this positive feedback by effectively modifying the inverter PLL characteristics with gain and / or phase shaping filters (see **Figure 10**). When S_{GRID} opens, the modified PLL reacts to any miniscule deviation in island frequency by introducing a slightly larger shift in the frequency of the inverter current. The island voltage mirrors this larger shift in frequency of the current which, in turn, further shifts the frequency seen by the PLL input. This process continues to further and further shift the island frequency until an under / over frequency protection limit is hit. When there is a strong grid connection, this positive feedback loop is broken because the PLL voltage input will be paced by the fixed grid frequency. One difficulty in these methods is finding the right balance of feedback strength: too little will result in failure to detect islands, but too much will result in reduced power quality or poor transient behavior if the grid fluctuates during normal operating conditions.

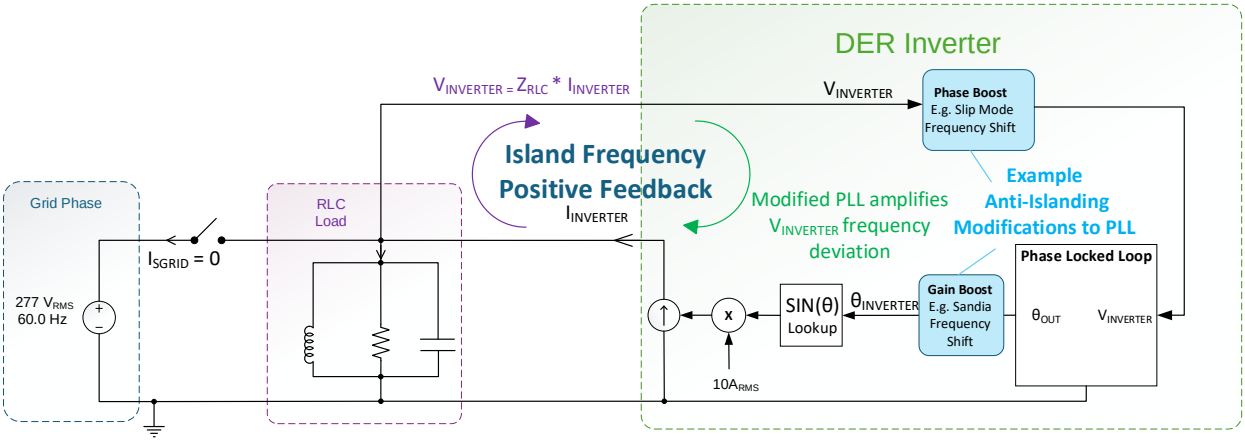

Figure 10. Illustration of positive feedback causing frequency runaway.

Impedance Detection

Another anti-islanding method involves measuring grid impedance and detecting an island condition e.g. if the measured impedance is above a certain threshold (see **Figure 11**). The grid impedance can be calculated by measuring the voltage resulting from a periodic test current (Bower & Ropp, 2002). Test currents may be non-harmonically related to the grid frequency to avoid harmonic interference from nonlinear loads. Test currents must be kept small to minimize additional stresses on the inverter and avoid excessive distortion in the line. Practical challenges include trying to coordinate the test currents when multiple inverters exist on the same segment. Multiple uncoordinated DERs on the same island will create uncorrelated perturbations that may reduce the effectiveness of this method.

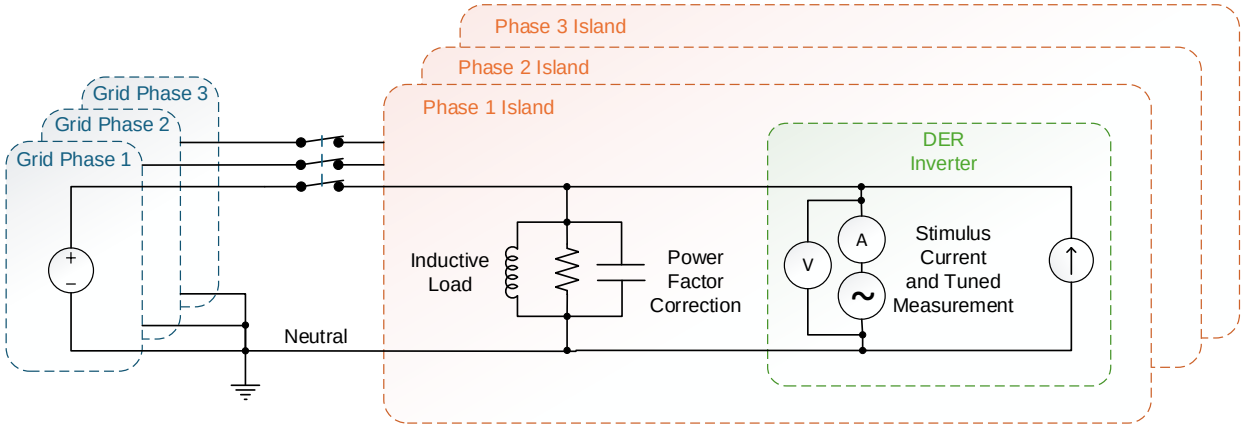

Figure 11. Measuring grid impedance to detect islands by injecting a stimulus current and making tuned voltage and current measurements.

Modulation of Reactive Power

A third category of anti-islanding algorithm modulates reactive power (see **Figure 12**). In the event of an island, this modulation will cause frequency ripple that can be detected by the DER. Under normal grid conditions, the extra reactive power cannot change the frequency of the grid, although, it does degrade the power quality of the DER. Finding the right balance of power quality degradation and island detection robustness is challenging. In addition, this method is susceptible to the issue of uncorrelated perturbations with multiple uncoordinated DERs.

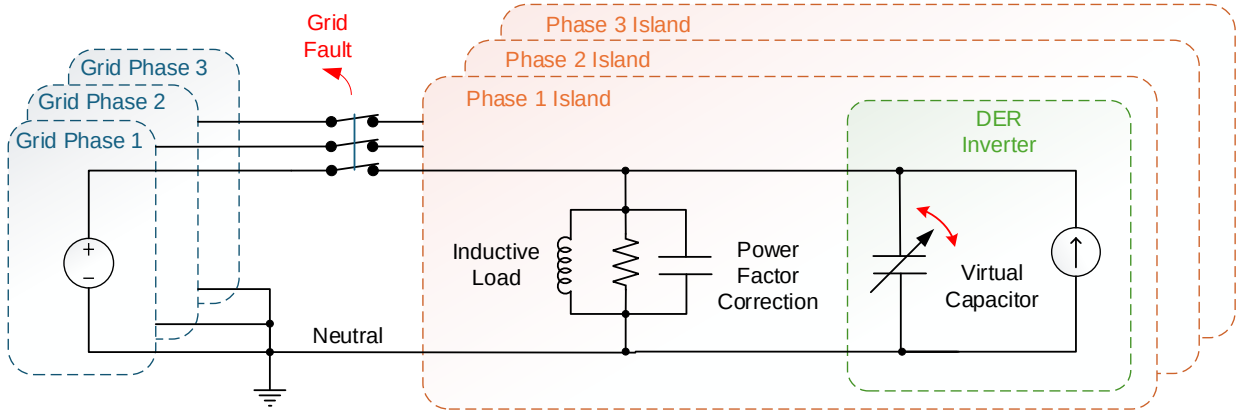

Figure 12. DER programmed to modulate reactive power like a virtual capacitor. Virtual capacitor acts in parallel with other capacitive loads to perturb the island frequency

$$F_{RESONANCE}(t) = \frac{1}{2 * \pi * \sqrt{L * C(t)}}$$

Equation 8. Modulating LC resonant frequency

Necessity of Standardized Testing

Certification to a grid standard such as IEEE 1547 by a Nationally Recognized Testing Laboratory (NRTL) serves as equipment acceptance testing when seeking permission from electric utilities to connect and export power to the grid. When an inverter model is certified for grid operation, it must pass a rigorous series of tests to ensure the robustness of the anti-islanding algorithm such that it will never pose a risk of forming an unintentional island. Because there are so many different forms of anti-islanding protection, each with their own strengths and weaknesses, and the DER is tested without knowledge of the internal inverter operation, there is no clear worst-case scenario to test. The robustness can only be demonstrated by means of many permutations of island scenarios. Unfortunately, performing this test suite has historically been very time consuming and labor intensive and has been a bane of testing for inverter manufacturers and certification laboratories for decades.

Unintentional Island Testing and Its Challenges

Increased Complexity in the Latest IEEE 1547 Standard

IEEE 1547.1-2020 is the compliance standard that defines many test procedures used to certify DER inverters before they can be installed and commissioned. Among these are the Unintentional Island testing, illustrated in **Figure 14**. The test setup is designed to emulate many permutations of real-world resistive, inductive (motors / transformers) and capacitive (power factor correction) loads and open-circuit grid faults in a lab setting. These adjustable island loads are used to verify that the inverter always detects and de-energizes the island in a specified period of time, typically 2 seconds.

Simple unity power factor islands represent only a small fraction of the test burden. Grid interaction standards, such as IEEE 1547-2018 have evolved to include different grid support functions intended to help stabilize the grid under adverse conditions (see **Figure 13**). DER active and reactive power can be modulated in response to deviations in voltage or frequency. Each of these functions affects the dynamics of island stability. To comprehensively evaluate an anti-islanding algorithm, IEEE1547.1-2020 Tables 13/14 define 10 grid support conditions which must be tested.

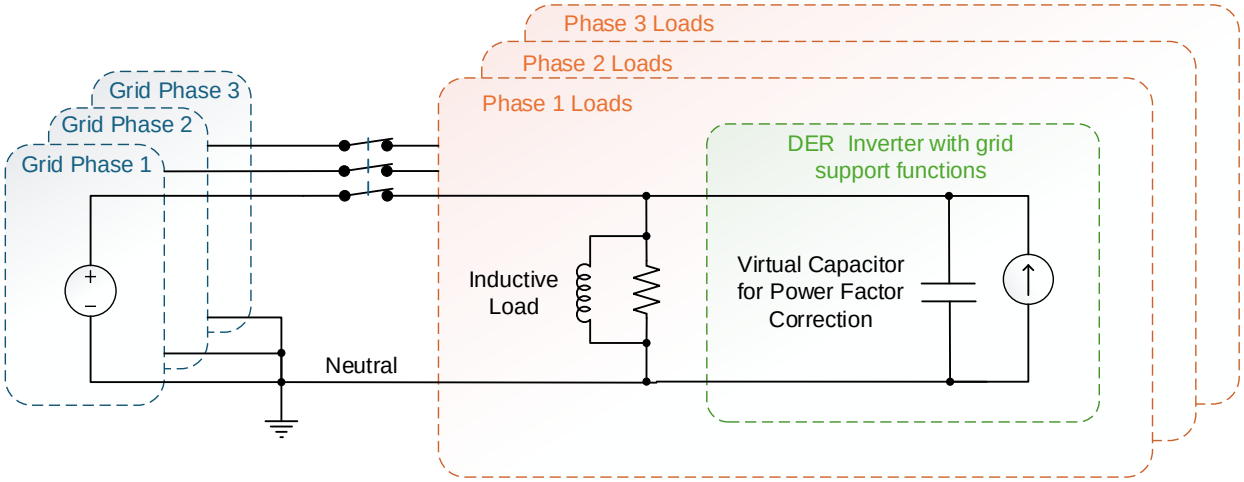

Figure 13. DER inverter programmed to provide reactive current for grid support acts like a virtual capacitor

Description of IEEE 1547.1-2020 Unintentional Island Testing Setup

For each prescribed grid condition, it is necessary to establish a stable island which serves as the control case for clearing time tests and verifies that the RLC loads have been properly tuned. Required anti-island clearing times are all 2 seconds or less, so an island persisting for 10 seconds is considered stable for the purposes of testing. First, the anti-islanding algorithm is disabled, and the island is tuned by measuring net grid currents with a variable RLC load in parallel with the DER. Next, the resistance is adjusted to absorb all real power from the DER. Then, the L and C are adjusted to absorb any reactive power in the system, and, also set up a tank with a Q-factor of 1. When residual grid current is < 2% of the DER current, a switch isolates the RLC load and DER from the grid. Island voltage, current, frequency and duration are measured on an oscilloscope or power analyzer and recorded. The flowchart in **Figure 15** illustrates this stable island test procedure.

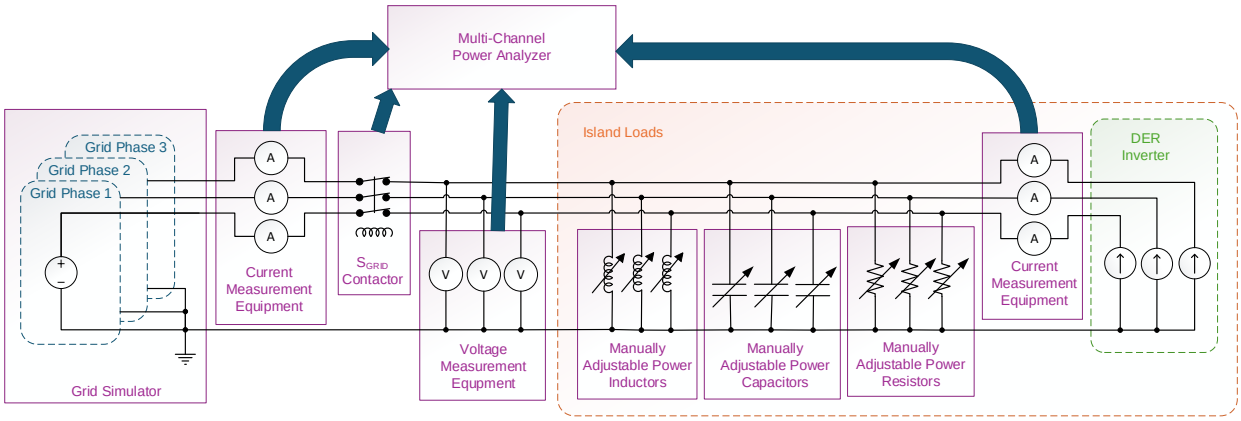

Figure 14. IEEE 1547.1-2020 test setup for performing unintentional island testing on a three-phase inverter. In the standard, S_{GRID} is referred to as "S_3".

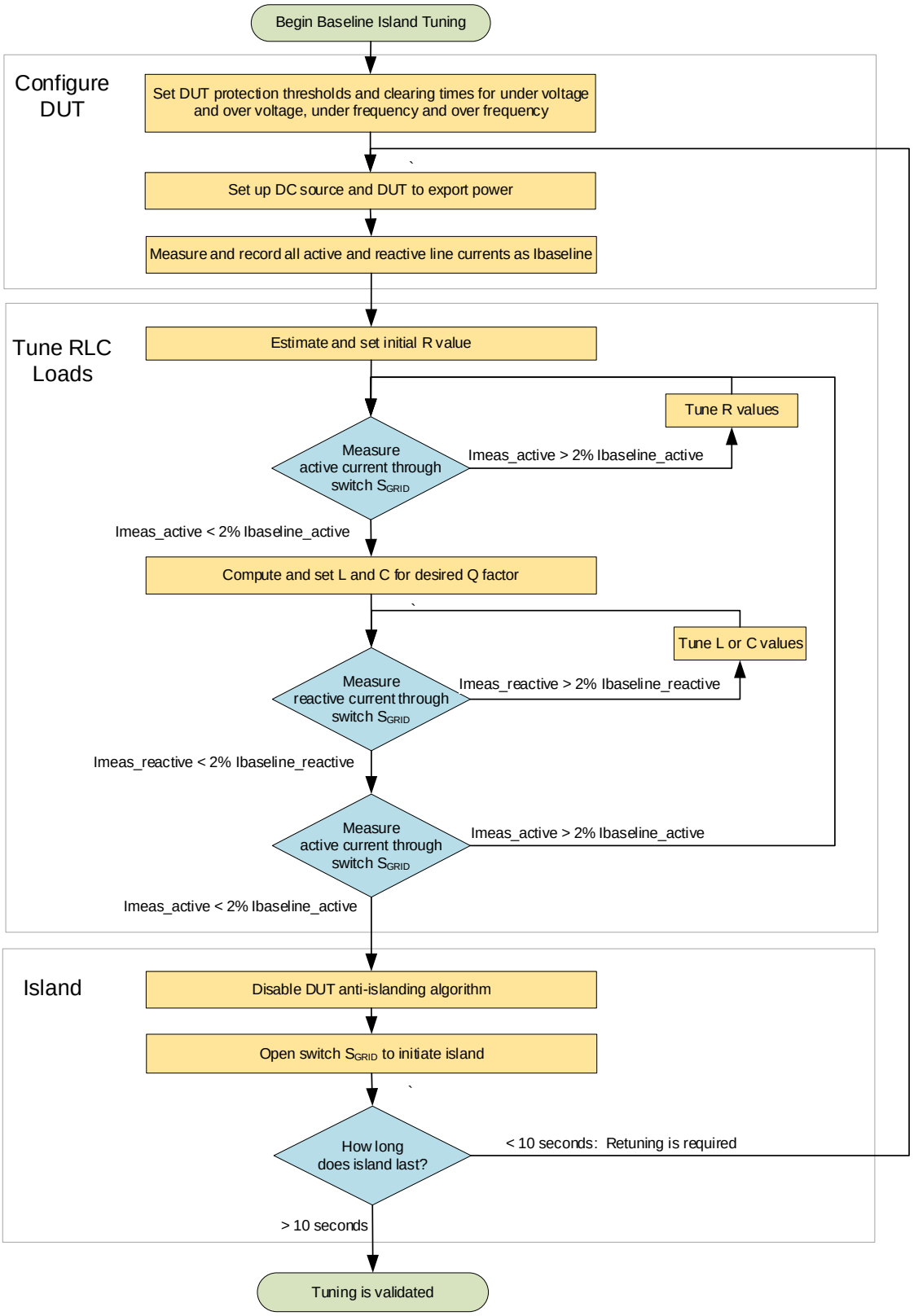

Figure 15. Baseline Island Tuning Flowchart, based on 5.10.2.2 c) and d) in IEEE 1547.1-2020

After the baseline island tuning has been established, the anti-islanding algorithm can be re-enabled, and the clearing time tests can begin. With the grid switch closed, and the RLC load unchanged, the DER is returned to its original operating point. Then the grid switch is opened to island the DER. The time elapsed between the beginning of the island and DER shutdown is measured and recorded. DER shutdown is defined as the point where the voltage and current waveforms drop below 5% of the initial values. This single iteration process is illustrated in **Figure 16**. To ensure the worst-case clearing time has been captured and that there are no Non-Detect Zones, the procedure is repeated from 95% to 105% of nominal reactive impedance (typically capacitive) with 1% steps until a trend of decreasing clearing times can be identified. Finally, the three tunings with the longest clearing time must be repeated twice more, totaling a minimum of 17 repetitions of the clearing time procedure for one test case and 170 repetitions for all 10 grid support conditions. If any of these iterations fail to de-energize the island within 2 seconds, the algorithm design must be corrected, and the test restarts from the beginning. **Figure 17** illustrates the clearing time test procedure for a single test case which must be repeated for each of the 10 grid support conditions.

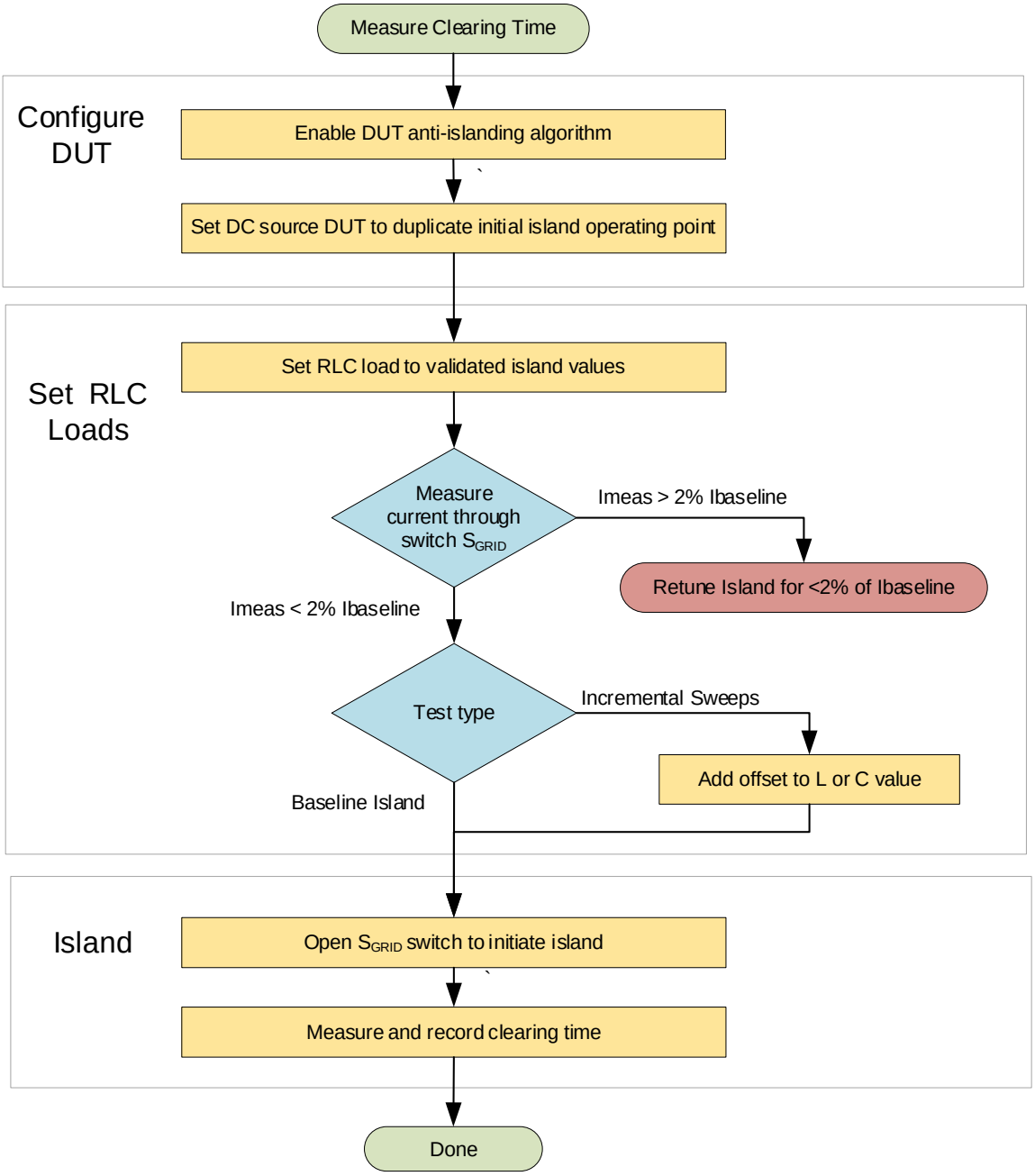

Figure 16. Clearing Time Test Flowchart based on 5.10.2.2 e) in IEEE 1547.1-2020

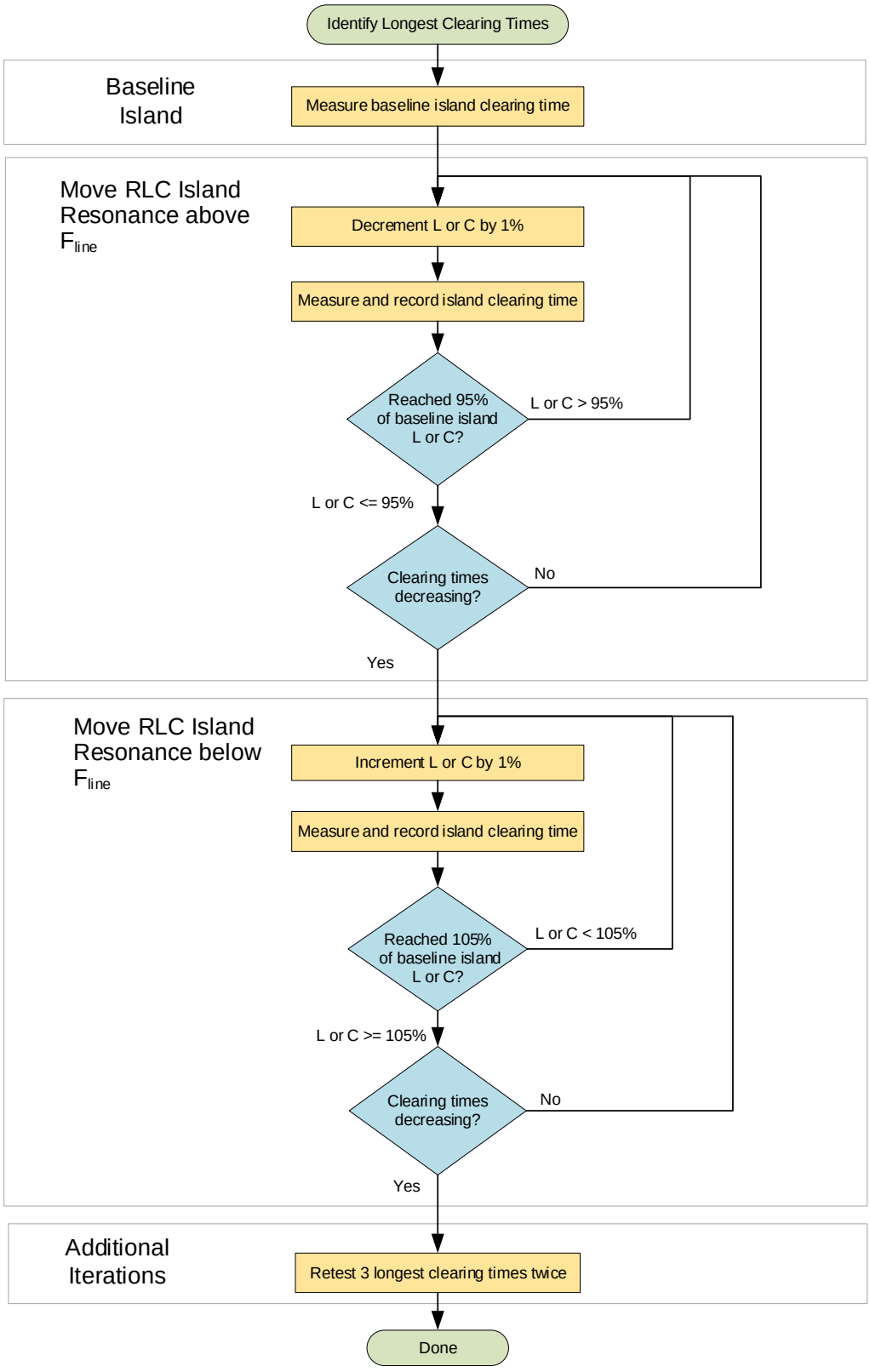

Figure 17. Worst Case Clearing Time Test Flowchart based on 5.10.2.2 e) in IEEE 1547.1-2020.

Challenges of Existing Test Methods

Loads and Range

Selecting and procuring the resistive and reactive loads is the first step in setting up an island test. High power resistors, inductors and capacitors are bulky, heavy and expensive. Some commercial RLC loads exist, but they are typically customized for a particular EUT or set of similar EUTs. Variable loads are not infinitely variable, so the practical range of achievable values or incremental adjustment is limited. Attempting to mechanically fine-tune large power components presents challenges for both test repeatability and manual dexterity. Accordingly, if a wide range of EUTs and power levels are to be tested, multiple sets of loads will be needed to reach the required impedances.

Heat Management

Resistive loads dissipate power, and heat management should be planned according to EUT size. A typical space heater is rated for approximately 1kW. Testing a multi-kW EUT with dissipative loads would quickly raise the temperature of a small test lab beyond the environmental limits of both the EUT and the operators. The total cost of dissipative resistive load solutions should be considered in the context of required support equipment. For large EUTs, it may be necessary to place the loads outdoors, or to upgrade building ventilation infrastructure to control the test environment.

Thermal Drift

In addition to the general operating environment, temperature changes of the resistive element itself will cause the resistance to vary according to the specified Temperature Coefficient of Resistance (TCR). This thermal drift will cause the tuned load current to change while the island test is in progress and make perfect power balance a moving target. Each test iteration begins by verifying that the S_{GRID} switch current is below 2% of the full operating current before attempting to island the DER. Waiting for temperatures to stabilize during every iteration is impractical, because it would dramatically increase test time, so thermal drift must be managed by aggressive cooling and employing power resistors made of specialized low drift alloys. Even still, a resistor with a TCR of 200ppm and a modest temperature rise of 50C would shift the load current by 1% - half of the total tuning error budget.

$$R = R_0*(1 + TCR*(T- T_0))$$

Equation 9. Resistance change with temperature.

Unwanted Couplings

Ideally, active and reactive current could be tuned independently, however several factors complicate this relationship. Although little current flows from the grid into the tank, for Q-factor of 1, the resonant current in the LC tank is equal in magnitude to the current flowing in the resistive branch. Power inductors suffer from magnetic hysteresis loss, eddy current loss, and copper loss. To a lesser degree, losses in capacitor dielectric also absorb real power. These parasitic resistances in the LC tank absorb active power from the DER and cause inconvenient couplings between the LC values and the expected resistance setpoint. Iterative tuning of all 3 parameters is usually required to reach the 2% residual grid current goal.

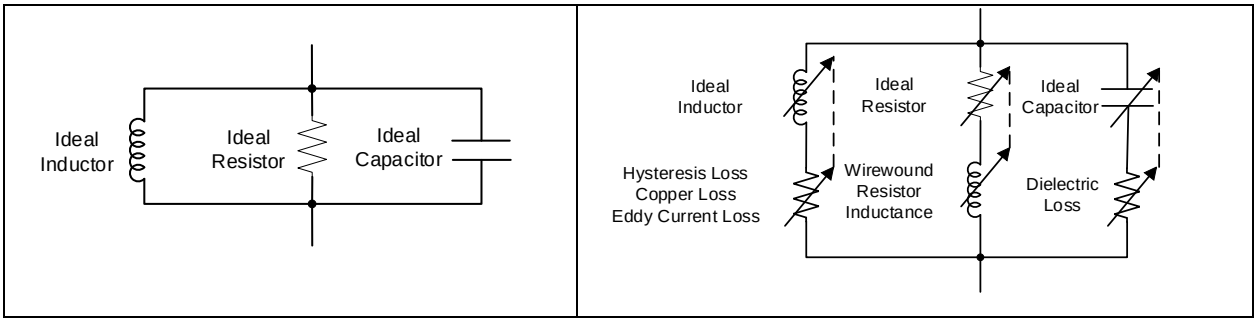

Figure 18. Idealized RLC load model vs. real load with coupled parameters and parasitic components.

Tuned Measurements

Basic reactive current measurements will capture more than just inductive and capacitive current. Active power factor correction standards such as IEC 61000-3-2 or IEC61000-3-12 permit a limited series of power line harmonics to flow into the grid, and inverter switching noise will also be measured as reactive current. Additionally, grid simulator voltage noise and non-zero harmonic distortion may excite reactive currents that flow in the pre-island circuit. Unlike active currents, where the residual grid current target is always zero, these harmonic and switching related reactive currents are always present, even with a perfectly tuned island. In a real test, frequency selective measurements are necessary and facilitate tuning by separating grid frequency current from other frequency content. This approach allows the test operator to confidently distinguish residual line-frequency reactive current, which can be reduced through island tuning, from the uncorrectable background of harmonics and noise.

Repeatability

Although IEEE1547 allows up to 2% residual current through the island switch S_{GRID} (S3), better tuning accuracy yields more repeatable results. A 2% residual current corresponds to a 2% impedance error on one branch of the load. If the S_{GRID} (S3)power is purely active, it causes a 2% island voltage error (for an EUT with unity power factor). For a 2% reactive current and a tank with quality factor =1, this residual current is enough to shift the island frequency by about 1% or ± 0.6Hz. This frequency variation is well outside normal operating conditions and can trigger grid support functions that further warp the island operating point.

Manual tank tuning for each of the 10 grid conditions and all their associated incremental test points is a tedious and time-consuming process. The test technician(s) must iteratively adjust the 3 coupled loads for each phase while using an oscilloscope or power analyzer to monitor the S3 current until it is below the 2% threshold. Repeatability and time required are heavily dependent on the skill and experience of the particular user or team operating the test. For the minimum of 170 test iterations, this test suite may take days or even weeks to complete, not accounting for issues or failures with the EUT.

Sailing through the Unintentional Island Testing with the SL1200 Series

The Keysight SL1200 series of grid emulators, along with the SL1200A Grid Integration and Compliance Test Automation Suite software package, allow automation of the unintentional island testing with an all-in-one instrument using built-in Power Hardware-in-the-Loop (P-HIL) technology, as well as a patent pending resonant RLC autotuning algorithm.

Reduced Footprint

The P-HIL technology allows the entire system: main grid, S_{GRID} switches (S3), power analyzers, and RLC loads to be simulated inside of the SL1200. There are no passive loads, relays, or external power analyzer involved, and everything is controlled programmatically. The amplifier power stages act as regenerative loads and return the energy to the building power system instead of dissipating it as heat. Even conventional P-HIL solutions require an external P-HIL simulator box and transducers. For the Keysight solution, the only equipment on the AC side of the inverter is the SL1200 series grid emulator (see **Figure 19**).

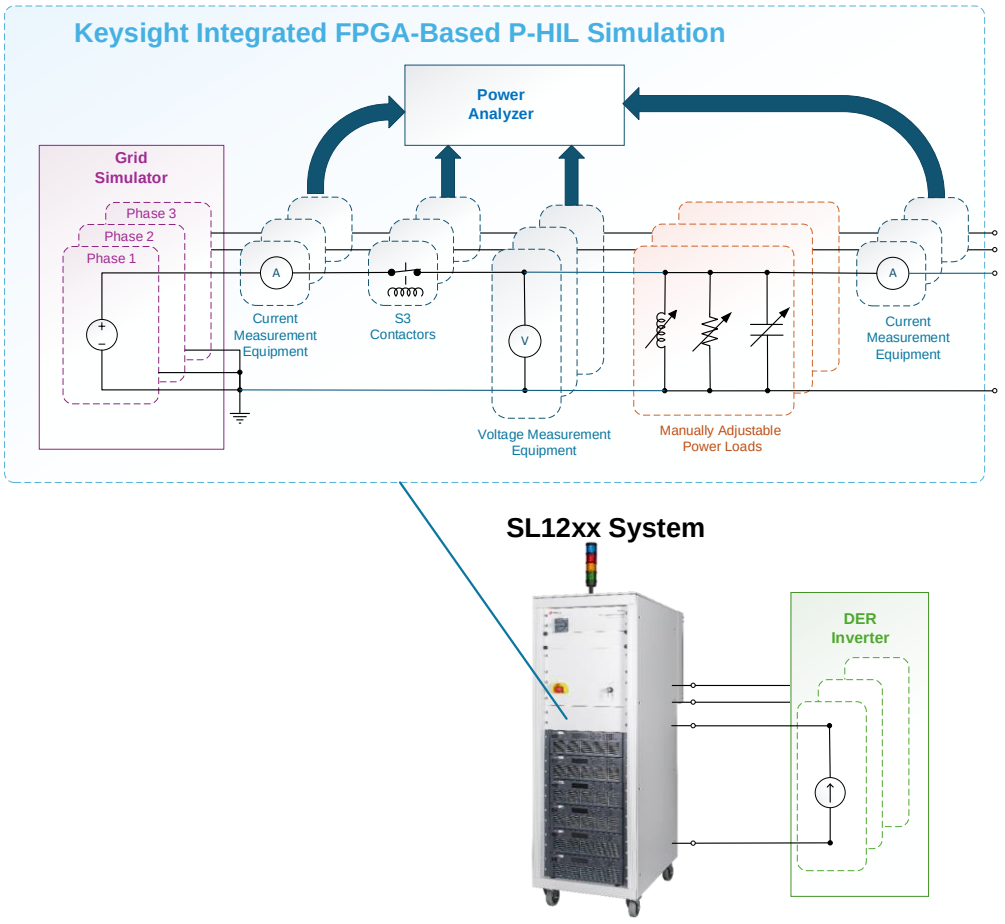

Figure 19. Diagram of test setup for Keysight solution with integrated grid and circuit simulation

Faster Test Time with Less Effort

The Resonant RLC autotuning algorithm creates a very precise, quick, and reliable way of tuning the RLC for each of the many test iterations. Filtered measurements based on fundamental frequency components averaged over several line cycles are taken to reject noise and fluctuations in line current. A tuned island with negligible S_{GRID} (S3) currents can be formed from scratch in seconds. This eliminates the need for a skilled user to perform manual tuning, enabling the unintentional island testing to be run with clicks of a button.

Repeatability

Automated RLC tuning can repeatably achieve S_{GRID} (S3) residual current below 0.2% and substantially reduce test variations from operator to operator and iteration to iteration. This performance is illustrated in **Figure 20** and **Figure 21**. Simplicity of the setup allows customer and NRTL to have identical setups, not just equivalent. This improved consistency helps the product design team debug the anti-islanding algorithm during product development and reduces the likelihood of surprises during NRTL certification. The same results are easily reproduced in any lab or site which has the Keysight test system.

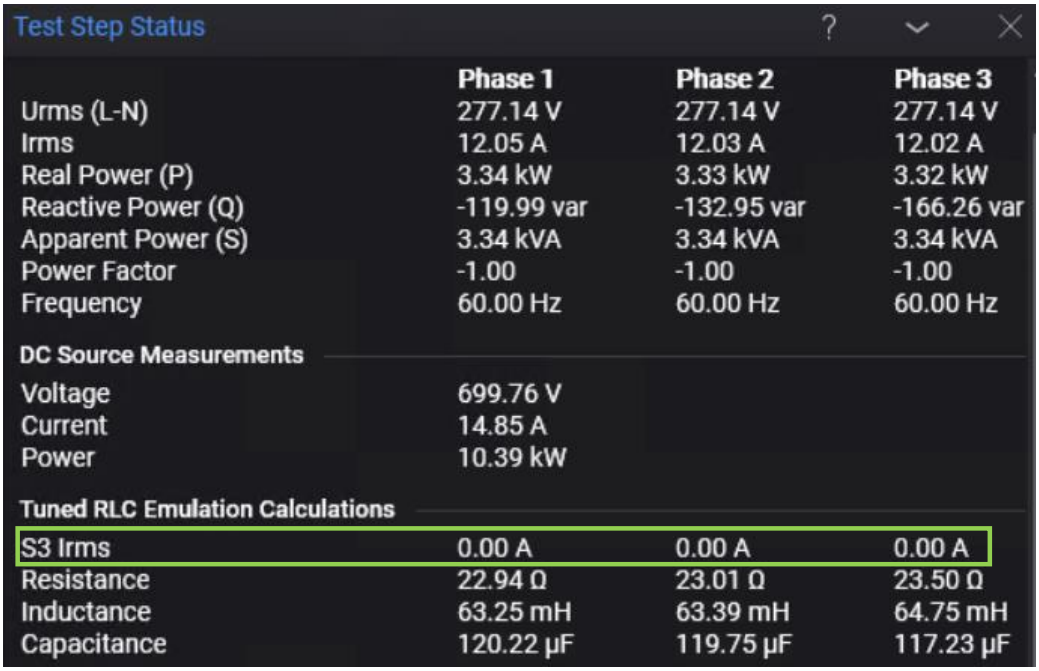

Figure 20. Software Test Status panel showing S3 measurements after automated tuning. All 3 phases are simultaneously tuned independently in a matter of seconds once the EUT is stabilized.

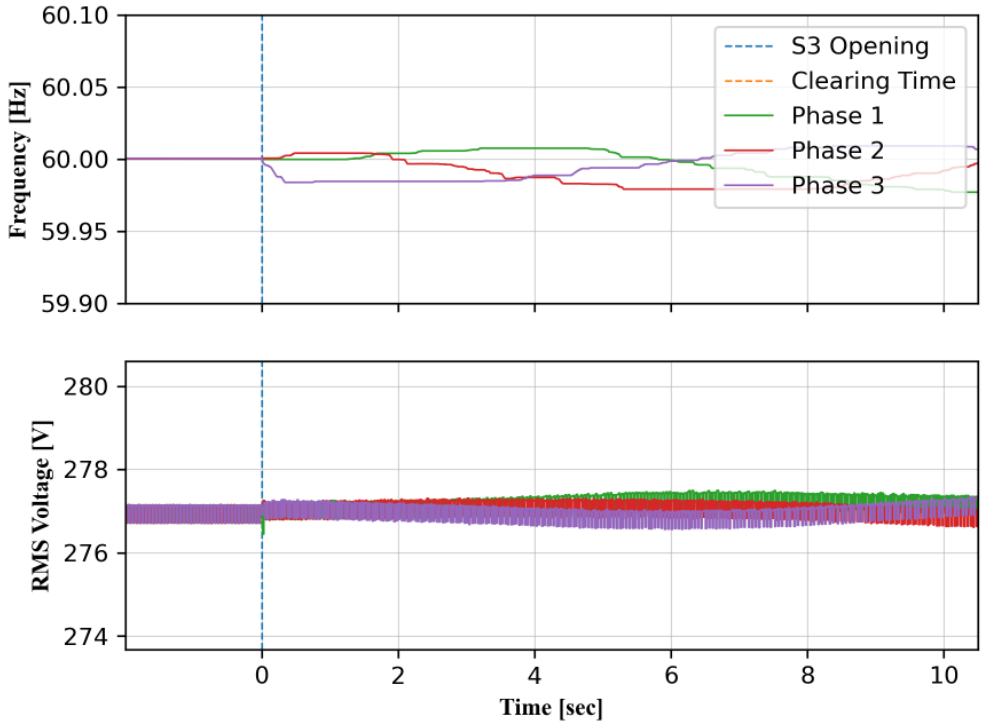

Figure 21. Sustained Island test waveforms with < 0.05 Hz drift in equilibrium frequency and < 1 V_{rms} drift in voltage, a result of tuning the RLC elements to < 0.2% error. This precision ensures the Keysight solution creates the most stable islanding conditions for the EUT anti-islanding algorithm to clear.

Out of the Box Solution

Other P-HIL solutions used in research and academia have been shown to perform the test without the use of passive RLC loads and S_{GRID} (S3) switches, but these setups require integration of a power amplifier, external simulator box, and current transducers. Careful examination of round-trip signal delays, characterization of the power amplifier and transducers, and feedback stability analysis by the end user are prerequisites to ensure a production-grade system. The Keysight solution is built-in to the fabric of the grid emulator, so all characterization is pre-verified in a single traceable firmware environment. The grid emulator and accompanying firmware meet the IEEE 1547.1-2020 unintentional island testing requirements for PHIL setups.

Built-in Software Analysis

The SL1200 grid emulator is controlled by the Keysight Test Automation Platform which displays test execution, allows customization of settings for development and debugging, and automatically computes clearing times. The SL1200A Grid Integration and Compliance Test Automation Suite software plots each incremental test point, establishes trendlines, and identifies maximum clearing times providing a concise visualization of the unintentional island testing results for the administrator and other invested personnel (see **Figure 22**, **Figure 23**, and **Figure 24**).

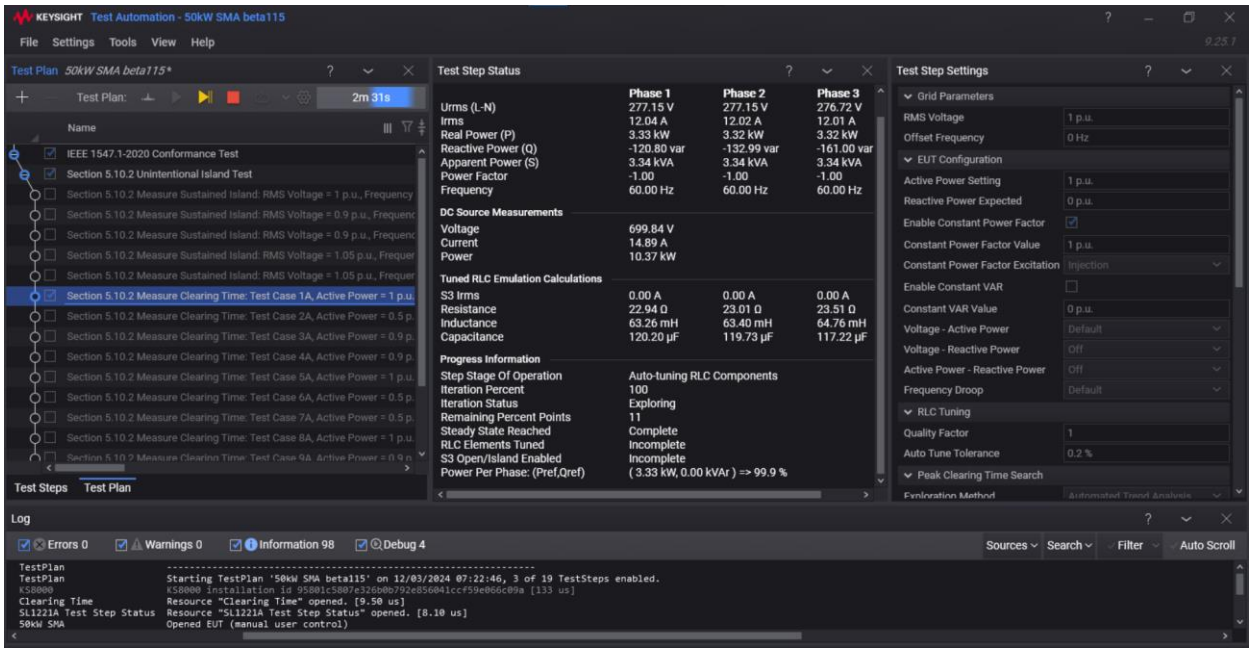

Figure 22. Unintentional Island testing software layout

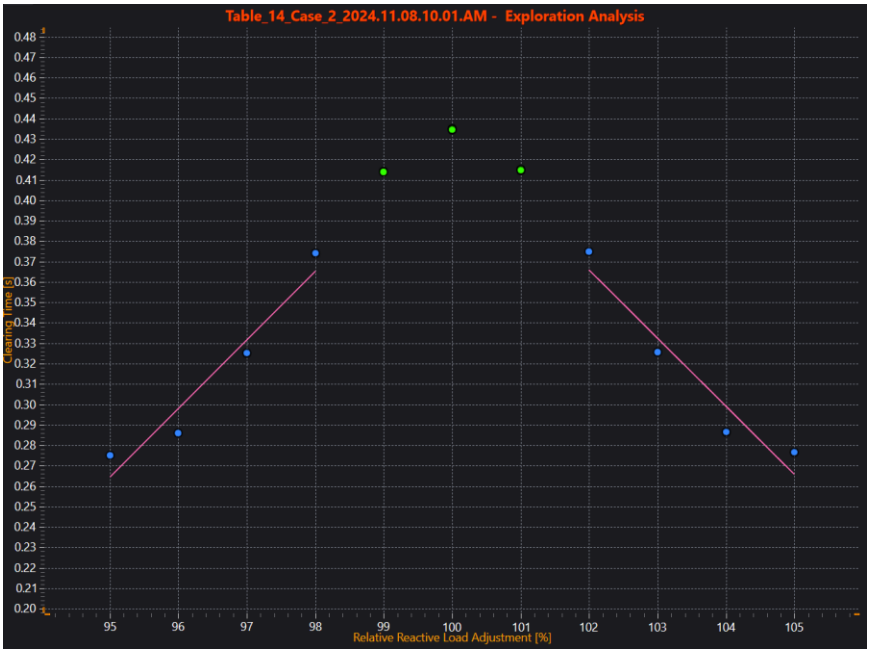

Figure 23. Runtime software analysis panel showing summary plot of test point, trendlines, and maximum clearing time of a test case

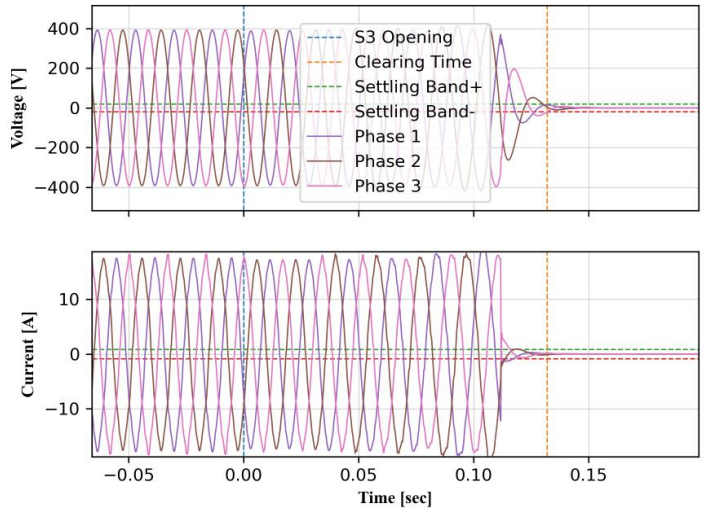

Figure 24. Post-processed results of EUT shutdown waveforms for a single run

Automated Test Report Generation

The SL1200A Grid Integration and Compliance Test Automation Suite software also provides a test report generator which aggregates the selected data, giving the user flexibility to focus on any subset of the test suite, ideal for both troubleshooting EUTs and producing final test reports. The unintentional island testing analytical report is illustrated in **Figure 25**.

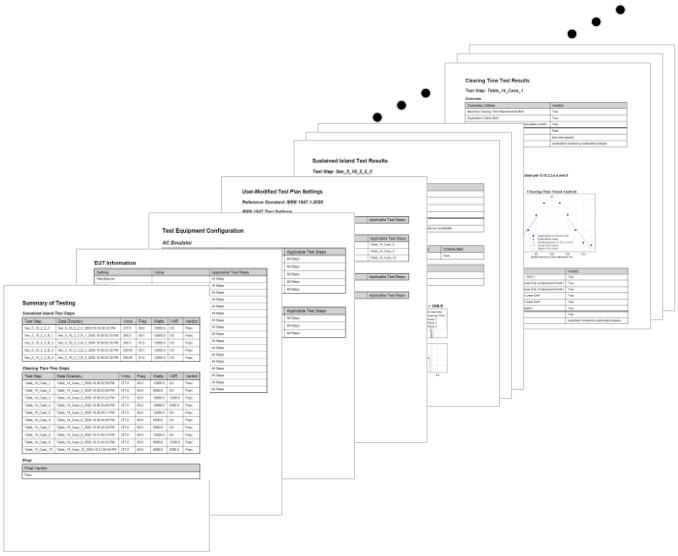

Figure 25. Test report automatically generated by software, complete with summary, verdict, configuration info, and analysis results.

Conclusion

Once the scourge of DER compliance testing, the unintentional island testing is a breeze with the Keysight SL1200 series of grid emulators and the SL1200A Grid Integration and Compliance Test Automation Suite software package. This solution combination reduces test time and manual labor and provides repeatability across sites. Automated analysis and reporting provide traceable results and eliminate the need for manual sifting through tabular data. Inverter manufacturers and NRTLs can now enjoy fast, consistent results and reduce this bottleneck for bringing renewable energy resources to our power grid.

FAQs

Q1

What is the difference between Stand-Alone Microgrids and Unintentional Islands?

Answer: Stand-Alone Microgrids can be considered stable and continuous intentional islands, separated from conventional power grids. They do not rely on an external connection for voltage regulation or power balancing. Unlike grid-tied DERs, microgrid equipment is designed to regulate its own voltage and match local power production to local demand.

Q2

What is the difference between active and reactive current?

Answer: Active current is the portion of current in phase with the voltage and the same frequency. It transfers real power between source and load. Reactive current is any current out of phase with the voltage. It includes 90 degrees leading and lagging currents from capacitors and inductors and also includes current at different frequencies such as line harmonics, interharmonics, and power converter switching noise.

Q3

Are resonant tanks common on the power grid?

Answer: At the frequency of resonance, inductive and capacitive currents are equal but opposite. These conditions exist not simply by chance, but by deliberate design in the form of power factor correction equipment. To prevent reactive current from consuming useful circuit capacity, capacitors are sized to supply a grid frequency current equal but opposite to the grid frequency current drawn by nearby inductive loads such as transformers or motors.

Q4

How is the SL1200 RLC emulation different from setting a phase angle on a conventional AC constant-current load?

Answer: Constant current loads with phase angle control can only approximate the behavior of an L or a C at a single operating point. The phase angle of an RLC tank varies up to 180 degrees with operating frequency and cannot be reproduced by constant phase angle equipment. Additionally, they are insensitive to changes in voltage and frequency, so system dynamics will be different than a real RLC load, especially under transient conditions. In contrast, the SL1200 RLC emulator multiplies the instantaneous current by a second order impedance model to accurately respond to changes in frequency and current and mimic the voltage and frequency dynamics of a physical RLC load.

Q5

Does the SL1200 use physical R, L, and C components for the island load?

Answer: No - the SL1200 is a bidirectional grid simulator. It emulates a programmable RLC tank using high speed power converters and control loops. When sinking power as a resistive load, energy is returned to the power grid instead of being dissipated as heat.

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