

# Keysight Technologies M9203A

## PXIe High-Speed Digitizer / Wideband Digital Receiver

2 channels, 12-bit, up to 3.2 GS/s,  
DC to 2 GHz bandwidth



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## Overview



## Introduction

The Keysight M9203A is a very fast and low noise PXIe High-Speed Digitizer/Wideband Digital Receiver featuring wide analog bandwidth, making it ideal for wireless, radar and satellite communication applications or any application requiring wideband signal capture with very high dynamic range. Thanks to its PCI Express® backplane connection, the M9203A supports continuous data streaming to disk.

## Product Description

The M9203A is a dual-slot 3U PXIe 12-bit High-Speed Digitizer/Wideband Digital Receiver running at up to 3.2 GS/s, with up to 2 GHz<sup>1</sup> instantaneous analog bandwidth and provides up to 4 GB of DDR3 acquisition memory. The M9203A features a large Xilinx Virtex-6 FPGA that can implement different functionalities depending on which firmware option you choose.

The M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver can also be combined with the **Keysight 89600 VSA Software** for advanced dual-channel signal analysis.

## Example Applications

- Wireless communication (5G, LTE)
- Emerging communication standards (e.g. DOCSIS 3.1)
- Radar and wideband signal capture
- Radar and satellite communication applications
- Semiconductor automated test

1. 2 GHz refers to the front-end bandwidth. The digitizer can operate in the 1<sup>st</sup> and 2<sup>nd</sup> Nyquist zones (using undersampling), but real-time bandwidth is limited by Nyquist to a maximum of [sampling rate/2], capped by the bandwidth option.

## Product Features

- 12-bit ADC resolution
- 2 channels (1 when interleaving with -INT option)
- Up to 3.2 GS/s sampling rate (with -INT option)
- DC up to 2 GHz input frequency range
- Up to 4 GB (1 GSamples/ch) of DDR3 acquisition memory
- 50  $\Omega$  input impedance, DC coupled
- Selectable 1 V or 2 V full scale range (FSR)
- $\pm 2\times$  FSR input voltage offset range
- $\pm 200$  fs channel-to-channel skew stability
- 15 ps RMS trigger time interpolator (TTI) precision
- Enhanced real-time processing using configurable Xilinx Virtex-6 FPGAs (requires -FDK option and appropriate FPGA software)
- High data throughput PCIe® Gen2 (x8) backplane
- Real-time digital down-conversion (-DDC option) on 2 phase-coherent channels
- Real-time digitizer raw data streaming and recording bundle (-CB0)
- Real-time digital down-conversion with I/Q data streaming and recording bundle (-CB2)
- Support for Windows and Linux

## Uncompromising Values

- Fast PXIe 12-bit wideband digitizer with on-board real-time processing
- Capture wide bandwidth signals
- High dynamic range acquisition for better measurement fidelity
- Accurate long term measurement
- Capable of switching between multiple firmware programs
- Self-trigger mode for unequaled synchronous noise reduction
- Open FPGA for custom processing
- Reduced test time by tuning and zooming on signals (-DDC option)
- Dual channel phase coherent streaming and recording with up to 320 MHz alias protected instantaneous bandwidth (IBW) via bundle -CB2

## Hardware Platform

### Hardware Overview

The M9203A is PXI Express compliant. Designed to benefit from fast data interfaces, the product can be integrated in PXIe and PXI Hybrid chassis slots. The PXI format offers high performance in a small, rugged package. It is an ideal deployment platform for many automated measurements systems.

### Block Diagram

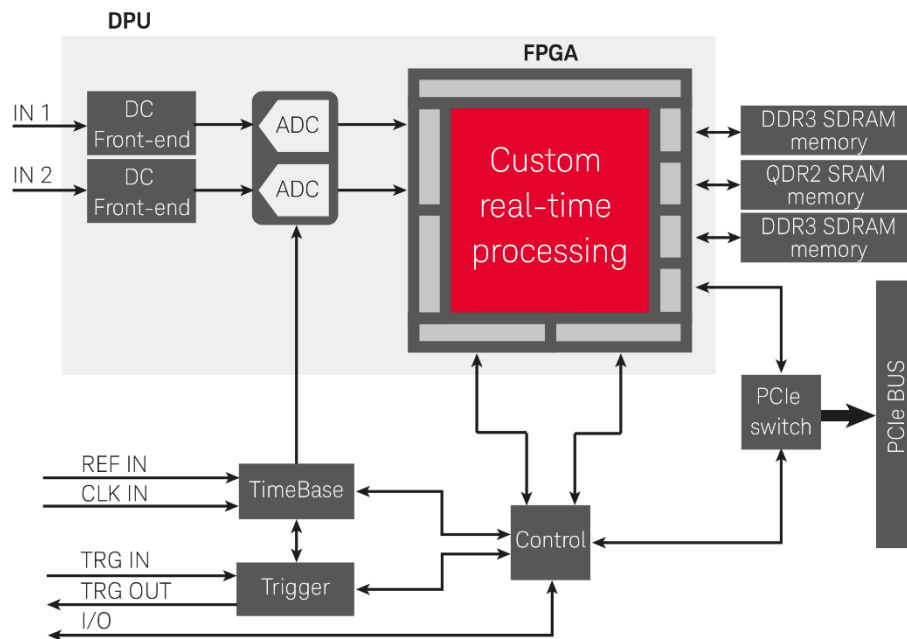


Figure 1. Simplified block diagram of the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver.

### On-Board Real Time Processing

At the heart of the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver is a data processing unit (DPU) based on the powerful Xilinx Virtex-6 FPGA. This DPU is responsible for controlling the module functionality, data flow and real-time signal processing. This powerful feature allows data reduction and storage to be carried out at the digitizer level, minimizing transfer volumes and speeding-up analysis.

The M9203A also provides open access to its on-board processing FPGAs for custom algorithm implementation using the -FDK option. This is achieved via the **U5340A FPGA Development Kit**, which can be used to implement custom algorithms.

The FPGA development kit is primarily intended to open the design of the FPGA to specific user requirements by providing a development framework that interfaces to the underlying hardware.

The FPGA development kit combines capabilities to:

- Achieve multi GS/s real-time processing on a full digitizer framework by leveraging the full density and speed of the FPGA.
- Shorten time-to-market with turn-key, easy-to-use development flow and debug.

There are several rationales to consider developing custom signal processing such as:

- Data throughput optimization
- Real time processing
- Implementation of custom IP and OEM technical know-how
- Re-usability and upgradability.

The FPGA development kit includes everything you need: source code, ready-to-use base design, a set of cores to easily interface to the underlying hardware, a test-bench environment for design and simulation, and automated building script.

For more information:

Keysight U5340A - FPGA Development Kit for High-Speed Digitizers

Keysight product brochure 5991-2424EN

<http://literature.cdn.keysight.com/litweb/pdf/5991-2424EN.pdf>

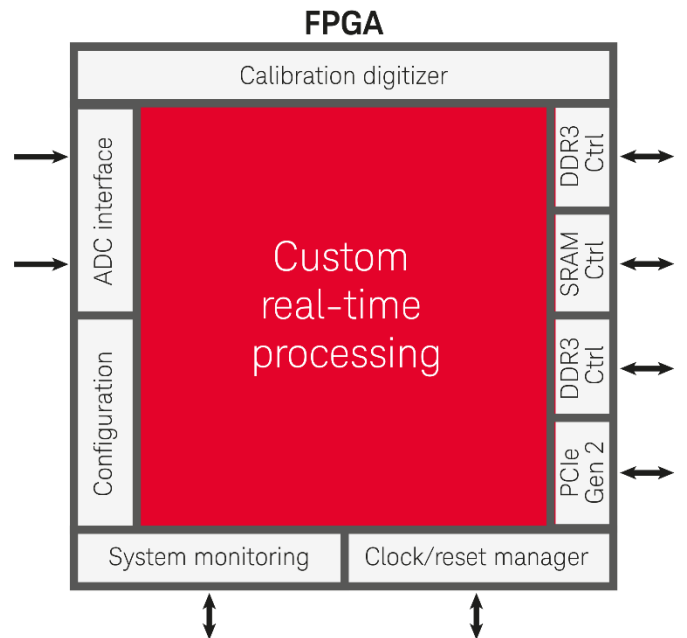


Figure 2. Enlarged block diagram of the FPGA Xilinx Virtex-6

□ Predefined Keysight IP Cores

■ Custom real-time processing (using FPGA development kit)

## Software Platform

### I/O Libraries

**Keysight IO Libraries Suite** offers fast and easy access to the M9203A digitizer using a standardized interface and ensuring compatibility and upgradability of the software applications.

The Keysight IO Libraries Suite displays all the modules in your system. From here you can view information about the installed software or launch the modules' soft front panel directly from Keysight Connection Expert (KCE). In addition, KCE offers an easy way to find the correct driver for your instrument.

### Drivers

The module comes with the IviDigitizer class compliant Keysight MD2 IVI-COM and IVI-C drivers that work in the most popular development environments including Visual C/C++, C#, VB.NET, MATLAB, and LabVIEW. Linux is also supported using the IVI-C driver.

### Easy Software Integration

To help you get started and complete complex tasks quickly, the M9203A PXIe Wideband Digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools to help you quickly develop test systems with your software platform of choice.

### Compliance

The M9203A is PXI Express compliant. Designed to benefit from fast data interfaces, the product can be integrated in PXIe and PXI Hybrid chassis slots.



Figure 3. M9203A front panel with analog inputs and multiple I/O signals.

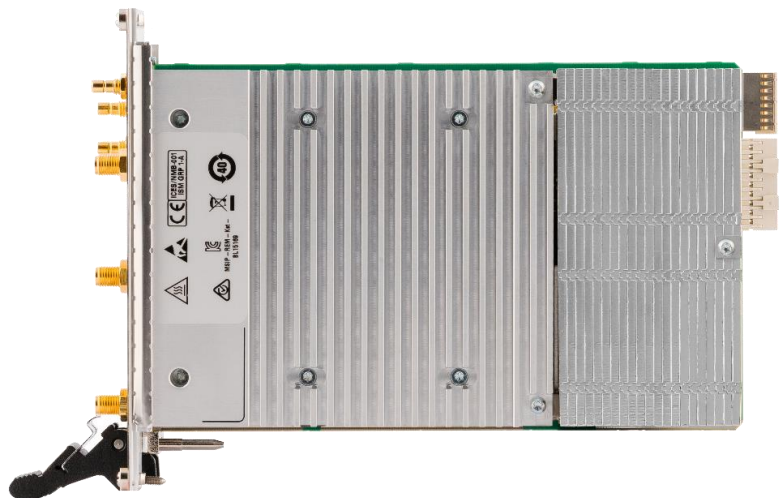


Figure 4. M9203A PXIe 12-bit High-Speed Digitizer/Wideband Digital Receiver offers a small size for easy integration within a PXIe chassis.



## Software Applications

In addition, the M9203A includes the Keysight MD2 soft front panel (SFP) graphical interface. This software application can be used to explore the capabilities of the Keysight modular high-speed digitizers.

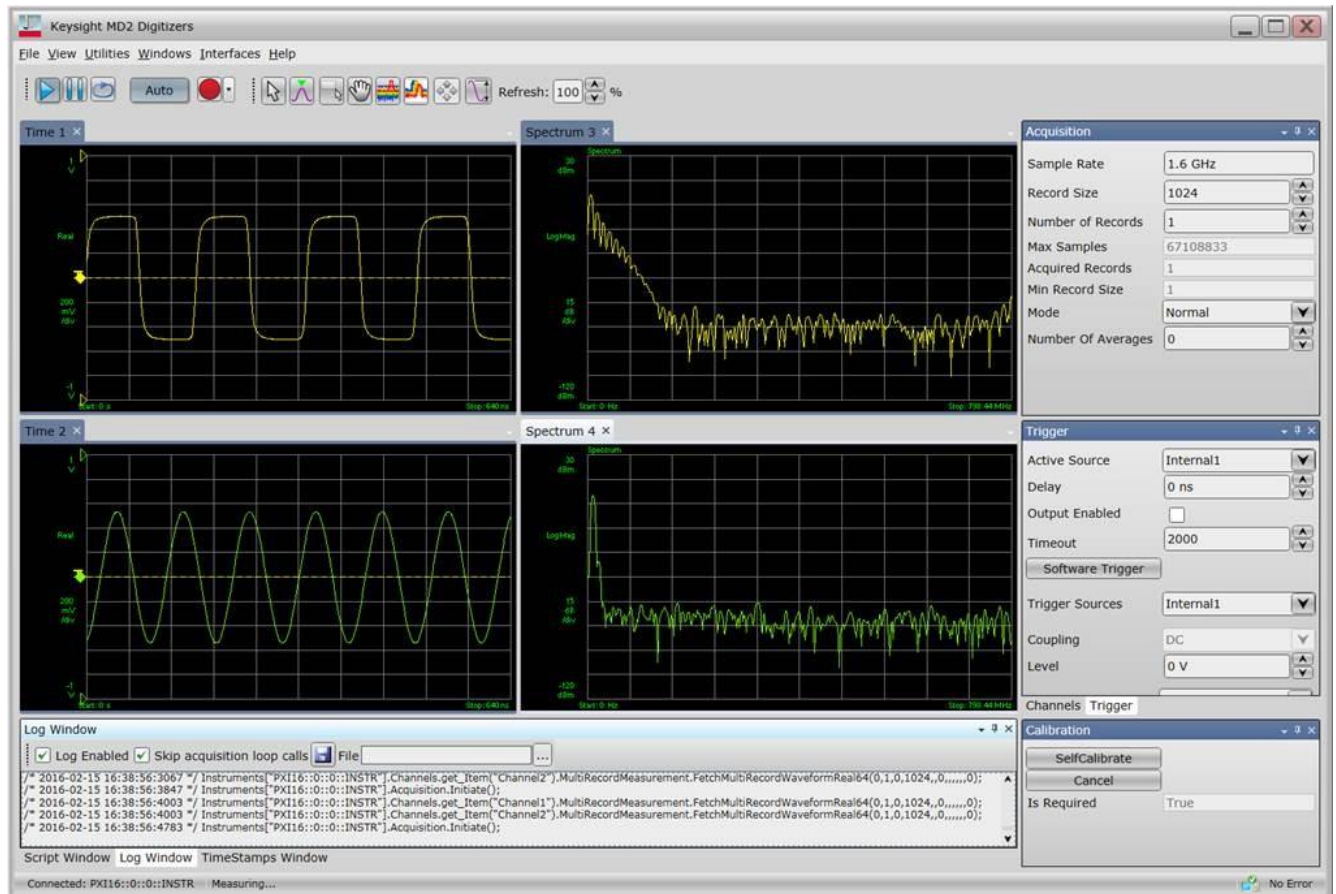


Figure 5. MD2 software front panel (SFP) interface.

The M9203A is also supported by the **Keysight U1092A Multichannel Acquisition Software**. This provides easy control and monitoring of advanced data acquisition systems with many channels, and is ideal for single-shot/event applications.

For advanced measurement analysis, the M9203A PXIe High-Speed Digitizer/Wideband Digital Receiver can be combined with **Keysight's 89600 VSA Software**, the industry's standard for signal analysis and demodulation. The M9203A allows fast connection to the 89600 VSA software through its high data throughput PCIe backplane, compared to traditional instruments.

## Firmware Options

The M9203A high-speed digitizer provides various firmware options<sup>1</sup>:

- DGT: Digitizer firmware
- INT: Interleaved channel sampling functionality
- FDK<sup>2</sup>: Custom firmware capability
- TSR<sup>3</sup>: Triggered simultaneous acquisition and readout
- DDC: Wideband real-time digital down-conversion

## Easy Firmware Switch

A simple call to the configuration function will switch the M9203A FPGA bitfile to the required option. e.g. Switching the loaded firmware from the -FDK option to the -DDC option.

## DGT Digitizer Firmware

This is the standard digitizer firmware which:

- Allows standard data acquisition, including: digitizer initialization, setting of acquisition and clocking modes, management of channel triggering for best synchronization, storing data in internal memory and/or transferring data through the backplane bus.
- Implements multi-record acquisition functionality.
- Supports fixed internal clocking frequency with internal or external reference, and variable frequency external clock.
- Offers programmable binary decimation to lower the sample rate by a factor of  $2^n$ , where  $n$  is an integer in the range of 1 to 10 for single record mode. e.g. Decimation from 1.6 GS/s down to 1.5625 MS/s.
- Trigger time interpolator (TTI): high precision integrated time to digital converter can be used to increase time measurement accuracy.

## INT Interleaved Channel Sampling Functionality

This interleave option allows two channels to be combined to reach 3.2 GS/s in one channel acquisition mode.

## FDK Custom Firmware Capability

This option enables the loading<sup>4</sup> of custom firmware created with the U5340A FPGA development kit<sup>5</sup>.

1. Firmware option functionality cannot be mixed when running a unit with multiple options, but they can be run one after another (i.e. the -DDC function cannot be used within the -FDK option, however the customer can develop his own DDC with the U5340A).
2. A calibration digitizer function is available with each firmware.
3. Only available with DGT option.
4. On the Virtex-6 LX195T DPU FPGA.
5. 11 W maximum power is dedicated to FPGA processing; the custom firmware design must fit within this power provision.

## TSR Triggered Simultaneous Acquisition and Readout

The TSR architecture allows the continuous acquisition of new records while reading previous ones.

Option -TSR is dedicated to applications requiring no trigger loss, achieving longer recording time when compared to the standard -DGT firmware.

Option -TSR main features:

- High trigger rate with guaranteed no lost triggers for specific configurations<sup>1</sup>.
- Easy to use solution, implementing an optimal and automated control of memory addressing.
- Larger memory size allows a longer record size and provides larger buffer for data transfer to host PC, especially useful for applications with non-periodic trigger or very high trigger rate during a limited period.

## DDC Real-Time Digital Down-Conversion

The real-time digital down-conversion option (-DDC), in addition to basic digitizer functionality, implements real-time digital decimation and filtering of the digitized data, allowing the user to tune and zoom on signals of interest. This exclusive IP algorithm provides very powerful and flexible digital down-conversion on all 8 channels. The filters and local oscillators (LO) are synchronized to maintain constant phase and timing relationships allowing phase-coherent post processing.

The -DDC option provides three main functions:

- Frequency shifting (tune)
  - Independently shifting the IF signal of each channel into baseband, allowing the analysis bandwidth to be set around the signal of interest.
- Data reduction (zoom)
  - Reducing the bandwidth and sample rate to match the analyzed signal, decreasing the amount of data that needs to be transferred for a given capture duration, which in turn accelerates post-processing operations.
- Magnitude trigger
  - Setting the magnitude level that the down converted signal needs to achieve at a specified frequency and bandwidth to generate a digital trigger on all channels.

These functions allow isolation of the signal of interest from other signals in a crowded spectrum, improving dynamic range as the integrated noise is reduced, and increasing both SNR and the effective number of bits (ENOB). The resulting advantage for your application is reduced test time, with improved overall test efficiency.

1. Please contact Keysight to find out the repetition rate that can be achieved in your application.

## Application Options

The M9203A high-speed digitizer can be configured with application specific options:

- CB0: Digitizer streaming and recording
- CB2: Digital down converter streaming and recording at 1.6 GS/s

### CB0 Digitizer Streaming and Recording

CB0 is a turnkey reference bundle, based on the continuous simultaneous acquisition and readout architecture, implementing a real time digitizer data recorder for gapless acquisition. It includes a command line application ensuring performance of up to 2 GB/s<sup>1,2</sup> in a specific qualified system. An easy to use data viewer application is also provided.

The -CB0 option is added to a pre-configured M9203A that consists of:

- 1.6 GS/s sampling rate (-SR2)
- Full bandwidth (-F10)
- 4 GB acquisition memory (-M40)
- Digitizer firmware (-DGT)

This streaming and recording bundle provides:

- Guaranteed recording specification<sup>2</sup>
- Data throughput optimization (12-bit, 10-bit or 8-bit mode).
- An intuitive command line application that is used to control the digitizer sampling rate and recording speed.
- A data viewer with a simple graphical user interface (GUI) that can be used to read, display, select, and export the data stored.



Figure 6. Streaming options (-CB0, -CB2) are proposed with a recommended host PC and SSD. Performance is guaranteed with specific configurations.

1. Equivalent to: 2 GS/s in 8-bit mode, 1.6 GS/s in 10-bit mode, and 1.3 GS/s in 12-bit mode.
2. Maximum streaming and recording performance is guaranteed using an additional qualified host computer system with a specific storage configuration. Keysight can supply and install this host computer system – please contact your local Keysight office for additional information.

## CB2 Digital Down-Conversion Streaming and Recording

This bundle enables continuous gapless acquisition, implementing:

- Digital down converter functionality in real time
- Data streaming to host
- Multichannel recording to disk of all I/Q samples for later analysis.
- Independent local-oscillators, with phase-coherency between channels.

The -CB2 option is added to a pre-configured M9203A that consists of:

- 1.6 GS/s sampling rate (-SR2)
- Full bandwidth (-F10)
- 4 GB acquisition memory (-M40)
- Digitizer firmware (-DGT)

This streaming and recording bundle provides:

- Guaranteed recording specification<sup>1</sup> up to 320 MHz, with tunable intermediate frequency.
- Data throughput optimization (I/Q samples with 32-bit, 16-bit or 12-bit mode).
- An intuitive command line application that is used to control the digitizer.
- A data viewer with a simple graphical user interface (GUI) that can be used to read, display, select, and export the data stored.

1. Maximum streaming and recording performance is guaranteed using an additional qualified host computer system with a specific storage configuration. Keysight can supply and install this host computer system – please contact your local Keysight office for additional information.

## Technical Specifications and Characteristics

### Analog Input (IN1 and IN2 SMA Connectors)

Number of channels		2 (without -INT option), 2 or 1 (with -INT option)
Impedance		50 Ω ±2 %
Coupling		DC
Full scale ranges (FSR)		1 V and 2 V (3.98 dBm and 10 dBm)
Maximum input voltage		1V FSR: Clamp at ± 3.6 V, absolute max. DC voltage rating ± 4.6 V 2V FSR: Clamp at ± 6.3 V, absolute max. DC voltage rating ± 5.0 V
Input voltage offset		-2xFSR to +2xFSR
Input frequency range (-3 dB bandwidth)	-F05, -SR2	DC to 650 MHz (nominal) in 1V FSR at 1.6 GS/s DC to 650 MHz (nominal) in 2V FSR at 1.6 GS/s
	-F05, -SR2, -INT	DC to 650 MHz (nominal) in 1V FSR at 3.2 GS/s DC to 650 MHz (nominal) in 2V FSR at 3.2 GS/s
	-F10, -SR2	DC to 1.9 GHz (nominal) in 1V FSR at 1.6 GS/s DC to 2.0 GHz (nominal) in 2V FSR at 1.6 GS/s
	-F10, -SR2, -INT	DC to 1.4 GHz (nominal) in 1V FSR at 3.2 GS/s DC to 1.4 GHz (nominal) in 2V FSR at 3.2 GS/s
DC gain accuracy		± 0.5% (nominal) in 1V FSR ± 0.7% (nominal) in 2V FSR
Offset accuracy		± 0.5% in 1V FSR ± 1.5% in 2V FSR
Time skew <sup>1</sup>	Channel-to-channel skew <sup>2</sup>	±50 ps (nominal) in same module ±150 ps (nominal) between multiple modules of same chassis
	Channel-to-channel skew stability <sup>3</sup>	±200 fs pk (nominal) 75 fs RMS (nominal) <sup>2</sup>
Bandwidth limit filters		650 MHz (nominal) for -SR2
Effective number of bits (ENOB) <sup>4</sup>		@ 410 MHz 9.1 (nominal)
Signal to noise ratio (SNR) <sup>4</sup>		@ 410 MHz 57 dB (nominal)
Spurious free dynamic range (SFDR) <sup>4</sup>		@ 410 MHz 64 dBc (nominal)
Total harmonic distortion (THD) <sup>4</sup>		@ 410 MHz -64 dB (nominal)

1. The channel-to-channel skew is defined as the magnitude of time delay difference between two digitized channel inputs, granted the same signal is provided to each channel at the exact same time.
2. The measurement represents the maximum time skew between 2 channels of a single unit, measured with a Sinefit method on 100 kSamples, for a sinusoid signal at 400 MHz and averaged 10 times.
3. Skew and offset stability are measured at 25 °C in a climatic chamber. The skew and offset between channels are measured every 5 minutes over 12 hours and after 1 hour stabilization time and the values represent the dispersion of the measurements.
4. Measured for a -1 dBFS input signal in internal clock mode with option -F10 at 1.6 GS/s (option -SR2).

Digital Conversion			
Resolution			12 bits
Acquisition memory (total)	-M02		256 MB (64 MSamples/ch); standard
	-M10		1 GB (256 MSamples/ch); option
	-M40		4 GB (1 GSamples/ch); option
Sample clock sources			Internal or external
Internal clock sources			Internal or external reference
	Maximum real-time	-SR2	1.6 GS/s
	sampling rates	-SR2, -INT	3.2 GS/s
	Sampling jitter		225 fs (nominal) <sup>1</sup>
	Clock accuracy		±1.5 ppm
External clock source (CLK IN SMA connector)			
	Impedance		50 Ω (nominal)
	Frequency range <sup>2</sup>	-SR2	1.8 GHz to 3.2 GHz
	Signal level		+5 dBm to +15 dBm (nominal), 0 V DC
	Coupling		AC
External reference clock (REF IN SMB connector)			
	Impedance		50 Ω (nominal)
	Frequency range		100 MHz ±1 kHz (nominal)
	Signal level		-3 dBm to +3 dBm (nominal)
	Coupling		AC
Acquisition modes			Single shot
			Sequence (multi-record) <sup>3</sup>
			Continuous

1. Jitter figure based on phase noise integration from 100 Hz to 1600 MHz.
2. The sampling rate corresponds to half of the external clock frequency in 2-channel mode (non-interleaved channels). In interleaved mode (only available with the INT option), the sampling rate corresponds to the frequency of the external clock signal.
3. Up to 131,072 records. Record maximum length = memory size/number of channels.

Trigger		
Trigger modes		Positive or negative edge
Trigger sources		External, Software, Channel
Channel trigger frequency range		DC to 250 MHz
External trigger (TRG IN SMB connector)		
Coupling		DC
Impedance		50 $\Omega$ (nominal)
Level range		$\pm 5$ V (nominal)
Amplitude		0.5 V pk-pk
Frequency range		DC to 2 GHz (nominal)
Maximum time stamp duration	-SR2	32 days
Trigger time interpolator resolution <sup>4</sup>		6.25 ps (nominal)
Trigger time interpolator precision <sup>4</sup>		15 ps RMS (nominal)
Rearm time (deadtime)	-SR2	500 ns (nominal)
Trigger out (TRG OUT SMB connector) <sup>1</sup>		1 (programmable), 50 $\Omega$ source
	Signal level	0.8 V <sub>pp</sub> $\pm$ 2.5 V <sub>offset</sub> (nominal) into high impedance
Control IO (I/O 1 and 2 MMCX Connectors) <sup>2</sup>		
Output functions		Acquisition active Trigger is armed Trigger accept resynchronization 100 MHz reference clock divided by 2 <sup>3</sup> Sampling clock divided by 32 <sup>3</sup> Low level High level FPGA synchronization
Input/output functions		FPGA programmable I/O

#### Real-Time Digital Down-Conversion (-DDC Option)

Acquisition modes		Basic digitizer or DDC digitizer <sup>5,6</sup>
Number of synchronous DDC channels		2 in a single module Up to 8 across 4 modules in the same PXIe chassis
Center frequency tuning range (LO)	-F10 -F05	DC to 1.6 GHz DC to 650 MHz
Center frequency tuning resolution		0.01 Hz
Independent channel center frequency tuning		Yes
Independent channel frequency span		No

1. At 10 MHz on a 50  $\Omega$  load.

2. I/O 3 reserved for future use.

3. Only on I/O 1.

4. At maximum sample rate or at decimated sampling rate down to 1/16 of the highest sample rate (1/32 of the highest sample rate with interleaving).

5. Real-time DDC is active only for the 1.6 GS/s sampling rate mode (non-interleaved mode).

6. In DDC mode, each sample is a pair of I & Q samples. Each sample is coded on 32 bits (16-bit I and 16-bit Q) for the highest decimated sample rate (i.e.  $n > 0$ ), otherwise the coding is made on 64 bits (32-bit I and 32-bit Q).



Environmental and Physical <sup>1</sup>		
Temperature range	Operating	0 to +50 °C (sea-level to 10,000 feet) <sup>2</sup> 0 to +45 °C (10,000 to 15,000 feet) <sup>2</sup>
	Non-operating	-40 to +70 °C
Altitude		Up to 15,000 feet (4,572 meters)
EMC		Complies with European EMC Directive <ul style="list-style-type: none"> <li>– IEC/EN 61326-1</li> <li>– CISPR Pub 11 Group 1, class A</li> <li>– AS/NZS CISPR 11</li> <li>– ICES/NMB-001</li> </ul> This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme à la norme NMB-001 du Canada.
Acoustic		European Machinery Directive Acoustic noise emission LpA < 70 dB Operator position Normal operation mode
Power Dissipation		
+ 3.3V	+ 12 V	Power on PXI connector
3.2 A (typical)	3.5 A (typical)	55 W (typical)
Mechanical Characteristics		
Form factor		3U/2-slot PXI-Express Chassis slot compatibility: PXI Hybrid, PXIe Front panel complies with IEEE1101.10 certification
Size		Length 185 mm x Width 130 mm x Height 40mm
Weight		0.8 kg (1.76 lbs)

1. Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.

System Requirements		
Topic	Windows	Linux
Operating systems	Windows 10 (32-bit and 64-bit), All versions Windows 8.1 (32-bit and 64-bit), All versions Windows 7 SP1 (32-bit and 64-bit) Note: If using high-speed digitizer applications DVD, Windows 7 (64-bit) is supported.	Linux Kernel 2.6 or higher (32 or 64-bit), Debian 7.0, CentOS 6
Processor speed	1 GHz 32-bit (x86), 1 GHz 64-bit (x64), no support for Itanium 64	As per the minimum requirements of the chosen distribution
Available memory	1 GB minimum <sup>1</sup>	As per the minimum requirements of the chosen distribution
Available disk space	2.5 GB available hard disk space, includes: <sup>2</sup> – 1 GB for Keysight IO Libraries Suite – 1 GB for Microsoft .NET Framework Note: 400 MB for high-speed digitizer applications.	100 MB
Display	Minimum of 1024 x 768, 96 or 120 DPI	No display required
Browser	Use a supported version of Internet Explorer; see <a href="https://support.microsoft.com/en-gb/help/17454/lifecycle-faq-internet-explorer">https://support.microsoft.com/en-gb/help/17454/lifecycle-faq-internet-explorer</a>	Distribution supplied browser

## Definitions for Specifications

**Specifications** describe the warranted performance of calibrated instruments that have been stored for a minimum of 2 hours within the operating temperature range of 0 to 50°C, unless otherwise stated, and after a 45 minute warm-up period. Data represented in this document are specifications unless otherwise noted.

**Characteristics** describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics are often referred to as Typical or Nominal values.

- **Typical** describes characteristic performance, which 80% of instruments will meet when operated over a 20 to 30°C temperature range. Typical performance is not warranted.
- **Nominal** describes representative performance that is useful in the application of the product when operated over a 20 to 30°C temperature range. Nominal performance is not warranted.

*Note: All graphs contain measured data from several units at room temperature unless otherwise noted.*

## Calibration Intervals

The M9203A is factory calibrated and shipped with a certificate of calibration.

Calibration is recommended every year in order to verify product performance.

1. On older PCs with minimum RAM, installation can take a long time when installing the IO Libraries Suite and the .NET Framework.
2. Because of the installation procedure, less disk space may be required for operation than is required for installation. The amount of space listed above is required for installation. The .NET Framework Runtime Components are installed by default with most Windows installations, so you may not need this amount of available disk space.

## Configuration and Ordering Information

### Software Information

Supported operating systems	See system requirements
Keysight IO libraries	Includes: VISA libraries, Keysight Connection Expert, IO Monitor

### Related Products

Model	Description
M9010A	10-slot PXIe Chassis, PCIe Gen 3
M9018B	18-slot PXIe Chassis, PCIe Gen 2
M9019A	18-slot PXIe Chassis, PCIe Gen 3
M9048A	PCIe Desktop Adapter, PCIe Gen 2 (x8)
M9021A	PCIe Cable Interface, PCIe Gen 2 (x8)
Y1202A	PCIe Cable, 2.0 m Long, PCIe Gen 3 (x8)
M9036A	PXIe Embedded Controller
M9037A	PXIe High Performance Embedded Controller
M9393A	PXIe Performance Vector Signal Analyzer: 50 GHz
M9362AD01	PXIe Quad Down-converter: 10 MHz to 50 GHz
U1092A-S0x	Keysight AcqirisMAQS Multichannel Acquisition Software
89601B	89600 VSA Software, Transportable License
U5340A	FPGA Development Kit for High-Speed Digitizers

### Accessories

Model	Description
U5300A-102	MMCX Male to BNC Male Cable, 1 m Long
U5300A-112	SMB Female to BNC Male Cable, 0.1 m Long
U5300A-110	XA110 SMA Input Overvoltage Protection Kit

### Typical System Configuration

Model	Description
M9203A	PXIe 12-bit Digitizer, 2 Channels
M9018B	18-slot PXIe Chassis, PCIe Gen 2
M9021A	PCIe Cable Interface, PCIe Gen 2 (x8)
Y1202A	PCIe Cable, 2.0 m Long, PCIe Gen 3 (x8)

## Ordering Information

Model	Description
M9203A	PXIe High-Speed Digitizer/ Wideband Digital Receiver, 12-bit, 3.2 GS/s, FPGA Signal Processing
	Includes: Software, example programs and product information on CD MMCX male to BNC male cable, 1m (qty 1)
<b>Configurable options</b>	
<b>Sampling rate</b>	
✓ M9203A-SR2	1.6 GS/s sampling rate version (3.2 GS/s sampling rate with -INT option)
<b>Bandwidth</b>	
✓ M9203A-F05	650 MHz bandwidth
M9203A-F10	Full bandwidth
<b>Memory</b>	
✓ M9203A-M02	256 MB (64 MSamples/ch) acquisition memory
M9203A-M10	1 GB (256 MSamples/ch) acquisition memory
M9203A-M40	4 GB (1 GSamples/ch) acquisition memory
<b>Firmware</b>	
✓ M9203A-DGT	Digitizer firmware
M9203A-DDC	Wideband real-time digital down-conversion
M9203A-INT	Interleaved channel sampling functionality
M9203A-FDK	Custom firmware capability
M9203A-TSR	Triggered simultaneous acquisition and readout
<b>Applications</b>	
M9203A-CB0	Digitizer streaming and recording
M9203A-CB2	Digital down-converter streaming at 1.6 GS/s
<b>Calibration</b>	
M9203A-UK6	Commercial Calibration Certificate with Test Data
M9203A-A6J	ANSI Z540-1-1994 Calibration
M9203A-1A7	Calibration + Uncertainties + Guardbanding (not Accredited)
<b>Recalibration Service Plans</b>	
R-50C-011-3	Calibration Assurance Plan - Return to Keysight - 3 years
R-50C-011-5	Calibration Assurance Plan - Return to Keysight - 5 years

✓ These options represent the standard configuration.

## Instrument Upgrades

Description	Upgrade number	Additional information
Bandwidth upgrade from 650 MHz to full bandwidth	M9203AU-F10	<b>Return to Keysight for upgrade</b>
Memory upgrade from 256 MB to 1 GB	M9203AU-M10	Customer installable license key
Memory upgrade from 1 GB to 4 GB	M9203AU-M40	Customer installable license key
Memory upgrade from 256 MB to 4 GB <sup>1</sup>	M9203AU-M10 M9203AU-M40	Customer installable license keys
Processing upgrade from option -DGT to option -DDC	M9203AU-DDC	Customer installable license key
Upgrade to enable Interleaved sampling	M9203AU-INT	Customer installable license key
Upgrade to allow FPGA programming (custom firmware capability)	M9203AU-FDK	Customer installable license key
Triggered simultaneous acquisition and readout	M9203AU-TSR	Customer installable license key
Digital streaming and recording	M9203AU-CB0	Customer installable license key
Digital down converter streaming and recording at 1.6 GS/s	M9203AU-CB2	Customer installable license key

1. Upgrading from 256 MB to 4 GB requires two upgrade licenses.

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