DATA SHEET

M9195B PXIe Digital Stimulus/Response Module

16-channel, 250 MHz, PPMU

KEYSIGHT TECHNOLOGIES

Overview

Experience high speed digital test capabilities at a whole new level. The Keysight Technologies, Inc. M9195B PXIe Digital Stimulus/Response (PXI DSR) module is ideal for IC design validation and production test environments. It goes beyond providing just standard capabilities. The new 16-channel, single slot PXI module introduces a high-performance pattern cyclizer for powerful pattern creation including advanced timing capabilities such as multiple drive edges per cycle. This provides flexible edge placement and stimulus/response delays for timing margin testing or cable length compensation. Additionally, it can support up to four independent multi-sites with an independent sequencer for each site.

Software tools included with the M9195B allow the user to modify vector and pattern parameters without requiring the user to recompile and download tests. An optional set of software tools include a graphical pattern editor and pattern conversion tools to speed test development by enabling test patterns from various EDA systems to be read in, edited, and output to the M9195B.

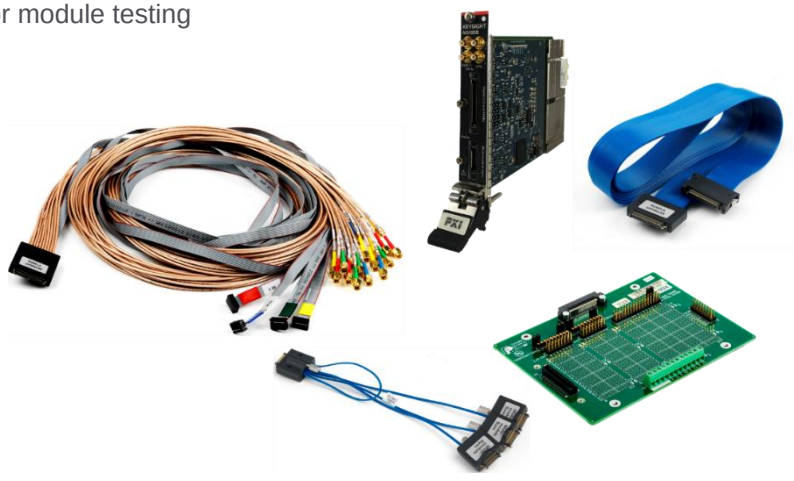
Additional ATE features include:

- High speed pattern application and RZ (Return-to-Zero) clock rate up to 250 MHz
- Per pin programming of voltage levels
- Real time compare, parametric measurement unit (PPMU)
- Deep vector memory and flexible pattern sequencing

With the PXI DSR module you can easily emulate standard serial interfaces like the MIPI® RF Front-End interface or proprietary parallel device interfaces. The test development software tools enable you to quickly create and edit waveform patterns or to import patterns created by automatic test generation applications.

Applications

- RFFE bus emulation used in PA/FEM semiconductor device verification or production test
- Wireless communication devices using parallel or serial digital control
- Automated test in product validation or manufacturing test
- Backplane emulation for device, board, or module testing
- Digital serial and parallel applications



Key Features

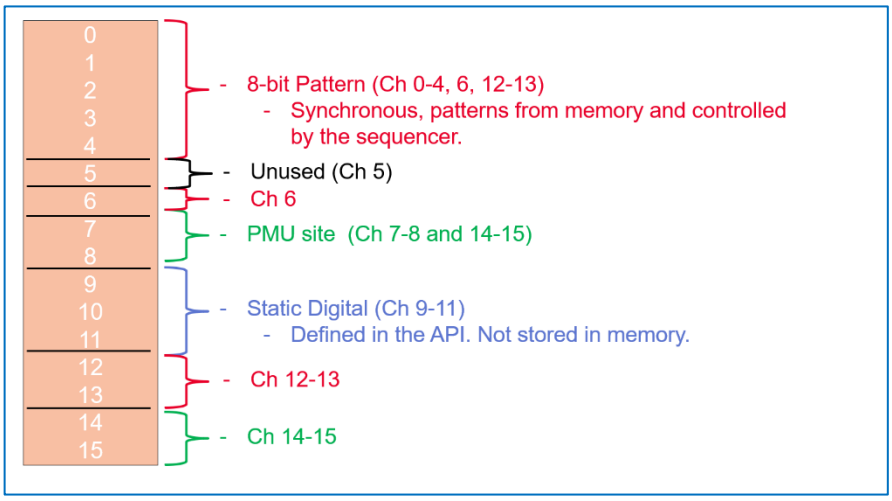
- Combine modules to form systems of up to 192 channels (requires option MMS)
- 16 bidirectional channels with per-pin programmable logic levels
- Highly flexible, per-bit timing control for fast and accurate waveform development
- Reconfigurable per-pin Parametric Measurement Unit (PPMU) for each channel
- Single and multi-site configurations
- Edit patterns on-the-fly without recompiling and downloading the test
- Execute patterns in arbitrary order
- Flexible allocation of deep pattern memory per channel or per site to allocate memory where it is needed
- Channel delay adjustment to compensate for cable and fixture propagation delays
- 4 high voltage channels for flash programming or fuse test
- 4 open drain auxiliary output pins for fixture relays
- Hardware triggers and markers for test system synchronization
- Comprehensive software tool set for quick test development

M9195B Hardware Overview

Individual channel capability

Each of the 16 bidirectional channels provide programmable logic levels of –1.5 V to +6.5 V with 152 µV resolution. The per channel 4 quadrant parametric measurement unit (PPMU) enables FVMI, FIMV, FVMV, and FIMI and FNMV modes. With the 5 PPMU current ranges between ±2 µA to ±40 mA, users can make accurate leakage measurements.

Each channel can be configured for parametric measurements, as a static digital I/O pin, or with synchronized cyclized digital data. This allows you to mix-and-match channels as required.



Digital channel direction and timing can be flexibly controlled on a per digital vector basis. The cyclized data allows each pin to operate in RZ or NRZ modes. In combination with the 1 ns edge placement resolution, each pin allows for an adjustable output delay, for timing margin testing, and receive delay to compensate for cabling propagation delays.

Memory Allocation

The M9195B normally allocates 125 Mvectors for each 4-bit channel bank (assuming option M12). If you are only using a small number of channels however, the sequencer will re-allocate the memory from the other banks using 4-bit wide sections. For example, if your pattern is only 1-bit wide, this will provide up to 500 MVectors of memory. This is an approximate value because memory is impacted by multiple settings.

To optimize vector memory, the following notes apply:

- You must use a flat-file (no loops) to maximize memory
- You must use a single sequencer with vectors which are four bits or less.
- All four channels must reside in the same channel bank
- You do not need M9195B-S04 (S04 does not provide any value in this case)
- Large files should be downloaded using “load bulk data deferred”
- You can increase the memory by an additional 5-10% if you are not using response vector memory (using stimulus vectors only).

Multi-site capability

The PXI DSR provides a choice of a single-site configuration with 16 synchronized channels, or a multi-site configuration with 4 sets of 4 synchronized channels. In multi-site mode, each site has its own independent sequencer. This enables site independent clock operation for simultaneous testing. The multi-site capability simplifies test development. Instead of forcing the test engineer to create a single test that encompasses all for sites simultaneously, the user only needs to focus on a single device. The single device test can be easily replicated for the remaining test sites. In addition to the digital pins, each site has a high voltage drive channel and an open drain control channel for relay control.

Multi-module synchronization

Up to 12 modules can be combined to build systems up to 192 channels (requires opt MMS for each module plus the appropriate sync cable, either Y1250A or Y1251A). When modules are combined, they operate in single-site mode and all channels are synchronized to a single test sequencer. Typical channel-to-channel skew (including across modules) is ±300 ps. Multiple modules are combined and programmed together into a single multi-module instrument.

Per-Pin Parametric Measurement Unit (PPMU)

The PPMU feature, available on each of the PXI DSR’s 16 channels, enables DC current and voltage measurements. Each channel can be independently programmed to force a voltage and measure the corresponding current or force a current and measure the voltage. The PPMU can make leakage current measurements at low current ranges or for measuring low input resistance in high current ranges. In a force voltage/measure current (FVMI) mode the PPMU can measure input bias current on a single DUT pin. For high current applications, each channel has remote sense capability to account for the voltage drop across the connecting cable.

Perform continuity testing of a DUT by forcing current into the pin with other DUT pins grounded while measuring the voltage at the pin (FIMV). The FNMV mode (Force Nothing, Measure Voltage) enables the PPMU to be used as a scanning voltmeter. The PPMU provides built-in 64 sample, 50 Hz or 60 Hz averaging to improve measurement quality by rejecting power line noise. All PPMU channels share a 16-bit measurement subsystem for fast accurate measurements.

Flexible digital pattern generation

With the included software tools, easily create, modify and reuse previously defined patterns. Pattern timing is controlled using up to 32 waveform tables. Within the waveform table, each of the 15 user-defined vector characters is translated into one of the following hardware actions: Force High/Low (U/D), Force to previous state (P), Stop Forcing (Z), Compare High/Low (H/L), Compare to Tri-state (T), Don't Compare (X).

Each vector period has two drive edges that are used when forcing a digital state and one receive edge used to compare digital data from the DUT. Edge placement resolution can be set as low as 1 ns and edge placement can vary from period to period so that oversampling is not required. The two drive edges enable the user to easily create a clock or other RZ formats from a single vector without requiring two vectors. The flexibility of the drive edges allow them to be changed on a per vector basis using the vector characters or by referencing a different waveform table.

The combination of the waveform tables and edge placement resolution simplifies the pattern programming. Variables and equations can be defined to allow the user to simultaneously modify timing relationships and edge placement.

Once compiled, the digital patterns are stored in the PXI DSR's on-board pattern cache. The PXI DSR executes the patterns from the cache in order to provide high test throughput. High-level pattern sequencing commands allow for high level macros which can be used to define timing sets, counted and uncounted looping of pattern blocks, conditional execution based upon matching parallel or serial patterns, or wait for software trigger advance.

Advance timing capabilities

Change pattern values that have been downloaded to the cache without recompiling. Pattern values can replace either parallel vectors or serial patterns. These powerful features allow you to quickly modify patterns directly from the API. The user can create pattern templates that are used to read or write to the DUT, then provide the vector information directly from the API.

Variables can be modified at the API level without recompiling the test pattern. This allows the user to control pattern timing or levels directly from the API. These advanced capabilities useful for test applications such as a timing or voltage level shmoo.

Serial and parallel digital bus emulation

The combination of the flexible pattern timing and sequencing features enable the PXI DSR to emulate a wide variety of standard or custom serial/parallel protocols such as SPI and RFFE.

Comprehensive Software Tool Set

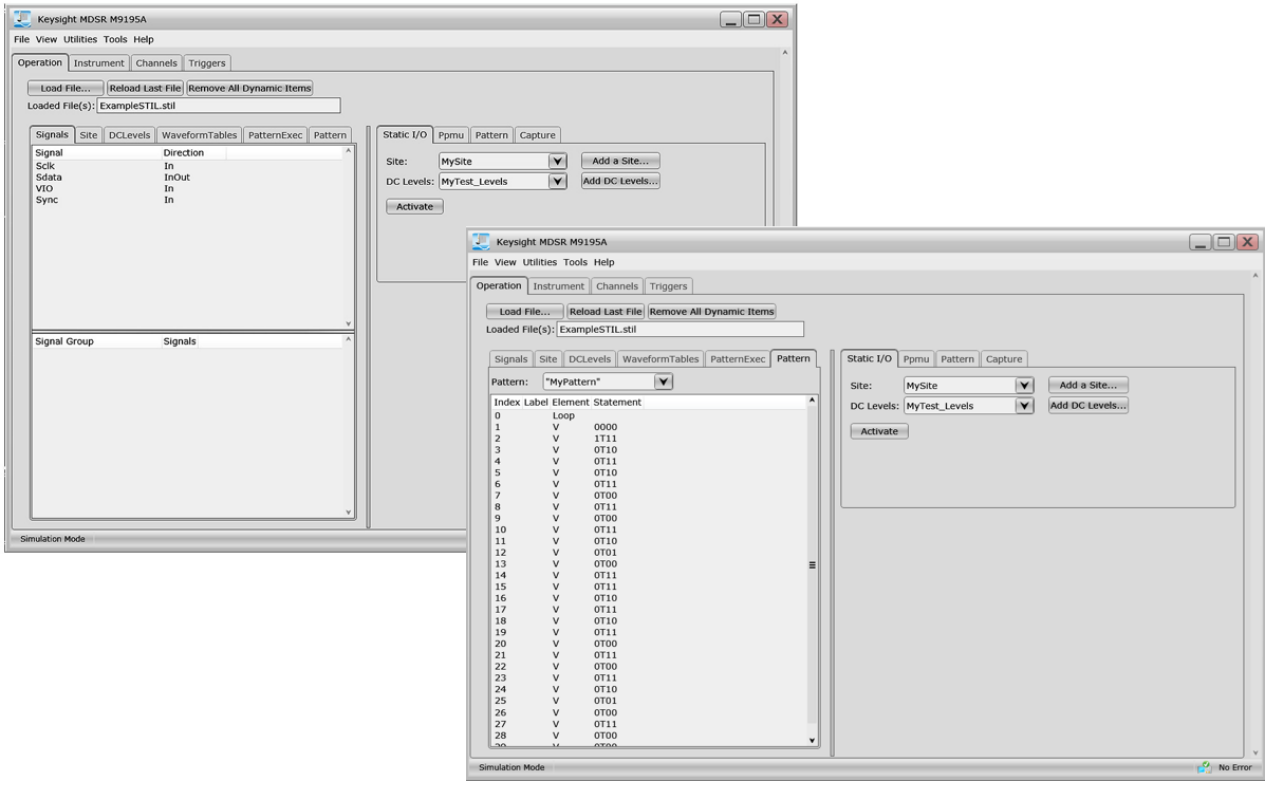
Keysight offers a choice of drivers and programming environments to configure and control the PXI DSR during test development including:

- Full featured, high-level IVI-COM, IVI-C, LabVIEW, and MATLAB programming interfaces through drivers
- IEEE-1450/ STIL, OpenXML (Excel), or text file format for programmatically defining patterns
- The M9195B Soft Front Panel for interactive test control and debug
- The M9192A/M9193A DSR pattern editor and data converters software enable test patterns from various EDA systems to be read in, edited, and output to the M9195B

These test development tools can be used in powerful combinations to match the DUT's test flow and test requirements.

Soft Front Panel (SFP)

The SFP assists the user in the development and application of test patterns, allows the user to change key test execution parameters, and allows the user to validate and compensate for test fixture connectivity. During pattern development, the user interactively loads and execute STIL, XML, or bulk data files. When loading, the tests are checked for correct syntax and the SFP generates error messages to help debug patterns. The SFP enables the user to the control various execution and response logging modes. In addition to these features, the SFP uses the same IVI interface driver calls. Each function initiated by the SFP logs an example driver call that can then be used in a regular API environment.



IVI and LabVIEW drivers

The IVI driver set can be used to fully control all aspects of test development using the DSR from assigning hardware pins to creating and executing waveform patterns using the M9195B. The drivers include high level commands for:

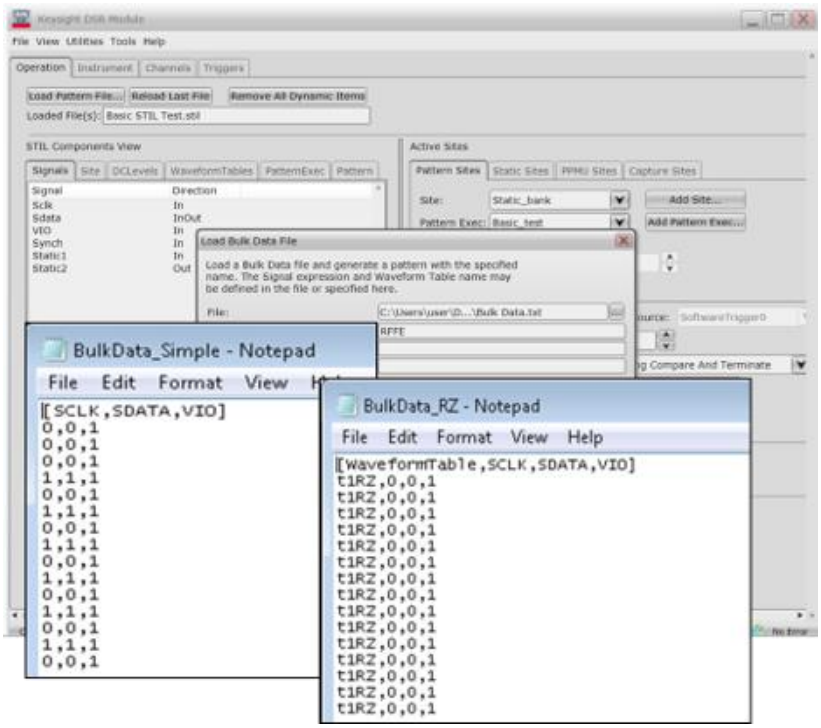
- Initial configuration including pin/channel names assignments, signal direction, grouping pins/channels to make vector definition easier
- Setting physical layer conditions such as voltage levels and active loads
- Defining single or multisite configurations.
- Pattern definition and waveform timing. Pattern sequencing

Standard Test Interface Language (STIL) support

The PXI DSR takes advantage of the Standard Test Interface language (STIL) IEEE Std 1450.0 which was designed for ATE testing. The PXI DSR can be configured using STIL commands that specify signal grouping, patterns, format, and timing information used to apply digital test vectors to a device being tested. Using a simple text editor and using the STIL format, attributes needed to generate digital patterns can quickly be created. STIL tests are easy to read and understand which simplifies test development and debug. Either the IVI API or the SFP can execute tests developed in STIL.

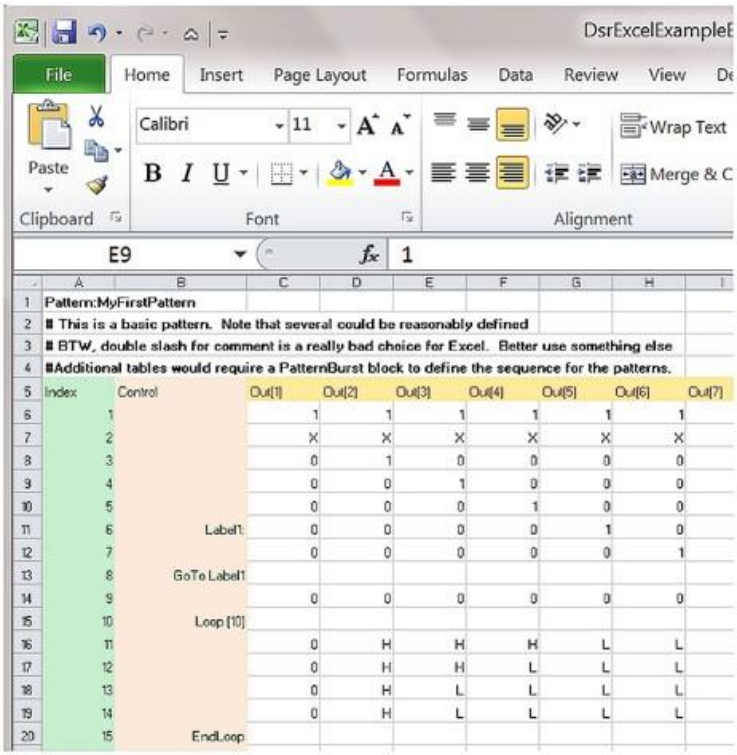
Bulk data import

The PXI DSR supports bulk data file import to load legacy and tool generated patterns. Bulk data import utilizes simple text files where the first row contains signal names and provides the option to a reference a waveform table. Each subsequent row represents the vectors which make up the patterns. The waveform table itself can be defined using the SFP, IVI driver, or STIL file. This provides a quick and easy way to develop production tests using patterns developed in R&D.



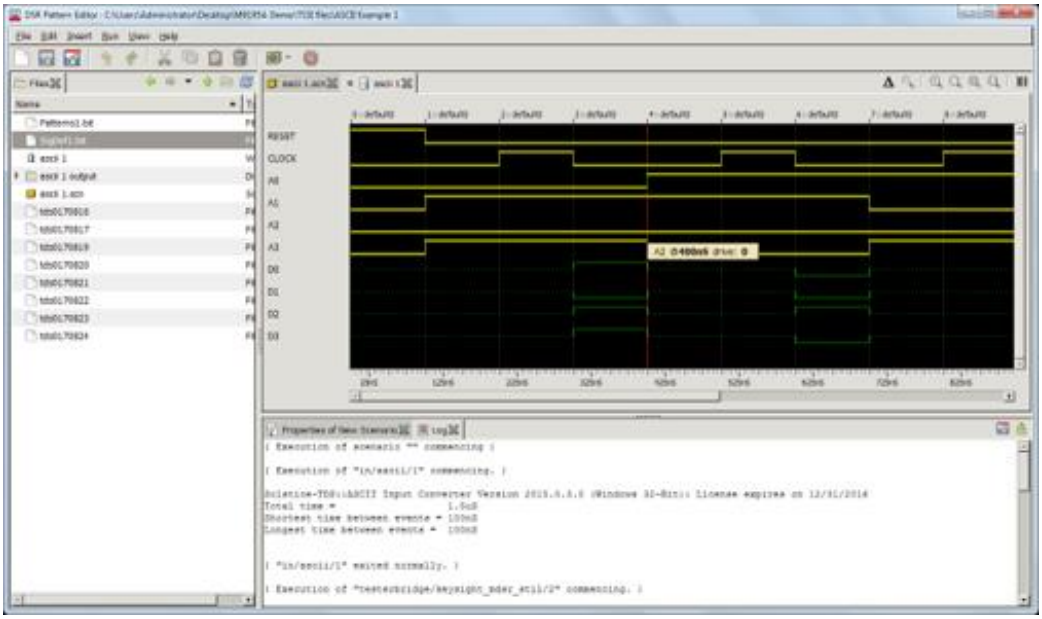
XML (.xlsx) programming interface

The XML interface allows the user to develop and debug tests in a spreadsheet form. The STIL methodology fits well with the multiple worksheet concepts provided in modern spreadsheet tools. Each worksheet matches a STIL function such as Signals, Waveform Tables, and Patterns. Digital patterns are tabular in nature and therefore fit very well into a spreadsheet. The spreadsheet provides an easy to use, flexible, and familiar interface for novice or expert users to quickly develop digital tests. All of the standard spreadsheet tools, such as equations, are available to help with pattern creation. This spreadsheet interface can be used to configure and control the M9195B channels and key features is provided as a standard development tool. Spreadsheet tests can be executed using either the SFP or associated IVI commands.



M9192A and M9193A DSR Pattern Editor and Data Converter Software

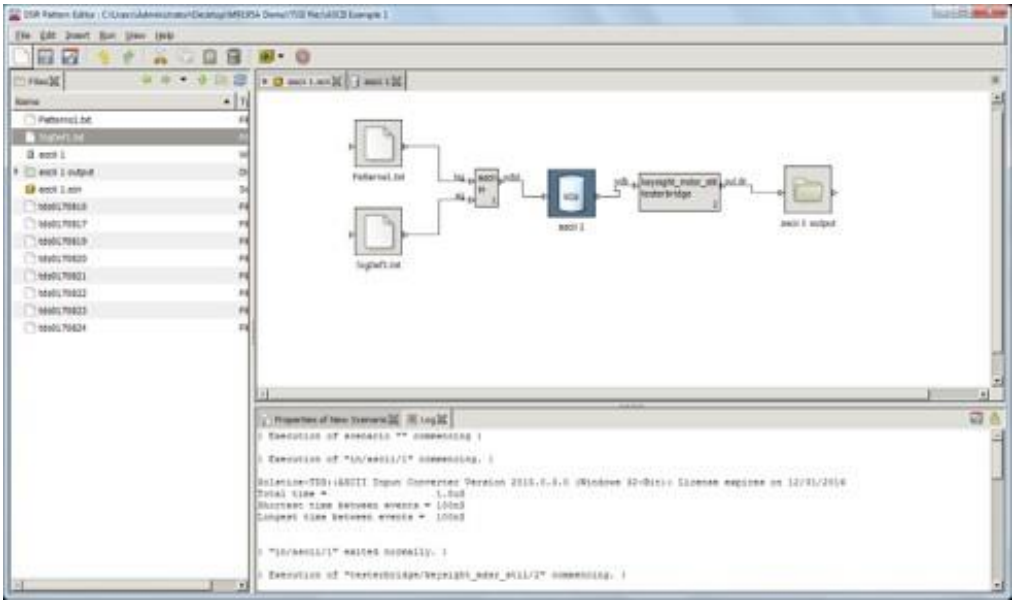
The optional M9192A and M9193A provide a complete set of vector translation and pattern validation software tools for the M9195B. These tools enable design and test engineers to save time, cut costs, and dramatically decrease time to market.



M9192A DSR pattern editor software

The M9192A DSR pattern editor, based on the Solstice-TDS WaveMaker+ module from Test Systems Strategies Inc. (TSSI), was customized to support the M9195B. The M9192A includes a DSR STIL In-converter, a DSR STIL Tester Bridge, and M9195B error handling. M9195B STIL files can be read using the In-converter and graphically displayed in the pattern editor. Patterns and timing information can then be edited in a single window. This enables you to generate and validate your own test patterns. The modified digital patterns can then be output as a STIL file utilizing the DSR STIL tester bridge. These STIL files can be loaded directly into the M9195B Soft Front Panel or used programmatically.

The pattern editor also speeds up test debug. M9195B error log files can be dragged-and- dropped into waveform editor. This gives immediate visibility of discrepancies between the expected and actual states of the DUT. The digital waveforms can then be edited to ensure a passing test.



M9193A DSR pattern editor with data converters software

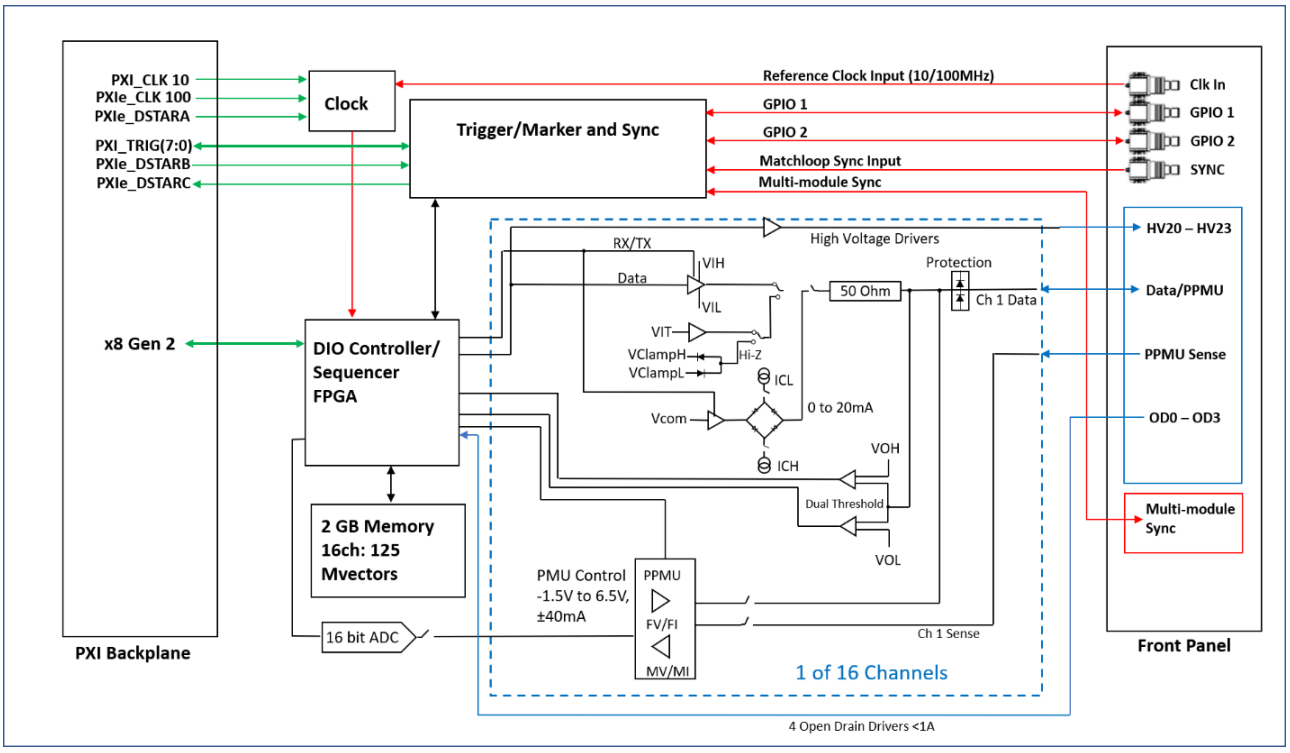
The M9193A DSR pattern editor with data converters combines the digital pattern editor with data converters based on Solstice-TDS In-converters from TSSI. The M9193A enables the utilization of digital pattern files from various Automatic Test Program Generators (ATPGs).

Vector files can be read using an appropriate In-converter and then edited using the pattern editor. In the case of Verilog files, an event-based database without timing is created when the VCE/ECVD file is read and supplied cyclization tools add timing. Once the digital patterns are complete, they can be utilized by the M9195B via the DSR tester bridge. The resulting digital development environment results in fast test development using ATPGs and customized output for the M9195B DSR.

The M9193A includes the following In-converters:

- The WGL In-converter reads an ASCII file that's compliant to the TSSI Waveform Generation Language (WGL) Specification.
- The STIL In-converter reads a text file that is STIL specification compliant (IEEE Std 1450.0-1999). This In-converter is very useful for reading files produced by many ATPGs including Synopsys TetraMAX, Cadence Encounter, and Mentor Graphics FastScan. Note: the M9195B PXIe DSR uses an enhanced version of STIL and is not supported with this STIL In-converter. However, the M9195B is supported with the Keysight DSR STIL In-converter that comes standard with the pattern editor.
- The Verilog In-converter converts a Value Change Dump (VCD) or an Extended Value Change Dump (EVCD) file generated by a Verilog simulator (e.g., Cadence IUS, Mentor Questa, or Synopsys VCS).
- The ASCII In-converter is a flexible, tabular form reader. The TSSI ASCII format is a host-independent, human-readable representation of cyclized test patterns. This format is designed for importing a bulk of data. The bulk data can be created from scratch or by converting from a different pattern format as long as it conforms to the TSSI ASCII format specification. Note: this data format is different than the bulk data format used with the M9195B Soft Front panel.

M9195B Block Diagram



Accessories and cables designed for easy, accurate, and reliable digital IO connections

Single-site (16 channels) signal cables

- Y1245A (0.5 meter), Y1246A (1 meter), or Y1247A (2 meter)
- 60 micro coax lines for 16 digital Ch, 16 PPMU sense Ch, 4 high voltage Ch, and 4 open drain/grounds Ch
- Male Edge Rate with squeeze latches or thumb screw hood

Multi-site (4 sites of 4 channels) signal cables

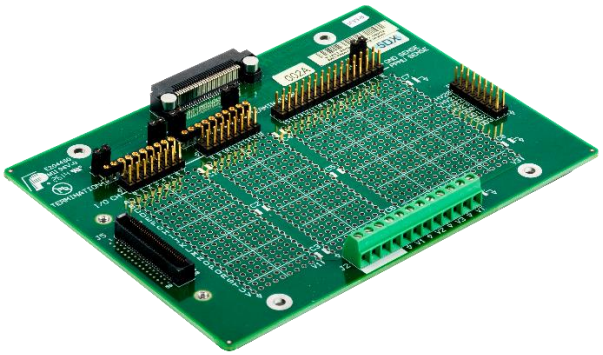
- Y1248A (1 meter) or Y1249A (2 meter)
- 16 Ch divided into 4 independent partitions (connectors)
- Each partition contains an Edge Rate connector with squeeze latch, 4 digital Ch, 4 PPMU sense Ch, 1 high voltage Ch, and 1 open drain Ch
- 4 alternate thumb screw hoods are also provided for optional use
- Requires option S04

Multi-module synchronization cables

- Y1250A four module cable or Y1251A twelve module cable
- Used to interconnect and synchronize multiple M9195B modules
- Only one cable is required per set of M9195B modules
- Requires option MMS

Evaluation and prototyping board

- Y1253A allows users to access individual signal pins for prototyping or debug.
- Board consists of 1 inch of signal header breakout pins, prototyping area with associated power connector, and signal termination pads.
- Offers 9 in^2 of bread board area, power/ground, includes headers for 16 channels, 16 PPMU channels high voltage and open drain channels
- The Y1253A proto board is designed for use with the single-site, Y1245A, Y1246A and Y1247A, cables only.



SMA Breakout cables

- Y1254A (1 meter) and Y1255A (2 meter)
- Enables user access to individual signal pins/channels for prototyping or debug
- SMA connectors plus a header for low-speed signals.
- Cables work with both the single and multi-site configurations

Technical Specifications and Characteristics

Definitions and Conditions

Specification (spec)
The warranted performance of a calibrated instrument that has been stored for a minimum of 1 hour within the operating temperature range of 0 to 45 °C and after a 30-minute warm up period. All specifications account for the effects of measurement and calibration-source uncertainties and were created in compliance with ISO-17025 methods. In addition, a driver session must be opened to initialize the power supplies. This can be done programmatically or by opening SFP and connecting to the instrument. Data published in this document are specifications (spec) only where specifically indicated.
Typical (typ)
The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty or calibration-source, and is valid only at room temperature (approximately 25°C).
Nominal (nom)
The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and applies room temperature (approximately 25°C). Data represented in this document are nominal unless otherwise identified.
Measured (meas)
An attribute measured during the design phase for purposes of communicating expected performance, such as amplitude drift vs. time. This data is not warranted and is measured at room temperature (approximately 25°C).
Additional Information
All data are measured from multiple units at room temperature and are representative of product performance within the operating temperature range unless otherwise noted. The data contained in this document is subject to change. To ensure proper cooling, use Keysight slot blockers (Y1212A), filler panels (Y1213A), and the air inlet module kit (Y1214A) in the chassis when there are empty slots. Keysight chassis and filler panels optimize module temperature performance.

General Characteristics

Module characteristics	
Bus interface and compatibility	PXIe peripheral module (x8 Gen 2)
Number of slots	1
Number of data/PPMU channels per module	16 (channels can either be configured as data or as PPMU)
Number of high voltage channels	4
Number of auxiliary open drain channels	4
Number of sites per module	One 16 channel or four 4-channel sites (option dependent)
Maximum data rate	250 Mbps (option dependent)
Maximum RTZ clock on data channels	250 MHz (option dependent)
Module memory (option dependent)	Up to 2 GB (allocated between pattern, response capture and sequence control)
Maximum number of synchronized modules	12 (requires option MMS)
Maximum number of synchronized channels	192 (requires option MMS)
Front panel connectors	
Data, open drain, HV, PPMU sense	ERCD30
Multi-module sync	ERCD10
Reference clock input (REF CLK IN)	SMB connector
Sync in/out (SYNC)	SMB connector
Trigger in/marker out (GPIO1/2)	SMB connector
Mechanical (nom)	
Size	3U/1-slot PXIe standard 130.1 x 21.7 x 210 mm; includes connectors and handle extensions
Weight	482g (1.1 lbs)

DC Power Requirements

DC supply	Typical	Maximum
DC supply current		
+3.3V	3.0 A	4.5 A
+12V	2.8 A	3.2 A
Power dissipation		
Total power dissipated	44 W	53 W

Data Channel Characteristics

Characteristic	Value	Comments
Number of data channels	16	
Maximum pattern memory	125 Mvectors per channel	Option dependent
Channel type	Single-ended, ground reference	
Channel impedance	50 Ω	Nominal
Direction control (In, Out, In/Out)	Per channel, per cycle (period)	
Per cycle digital states	2 drive states, 1 receive state	
Programmable drive states	Force high, force low, force terminate	Terminate state either drives active termination or is high-Z with reflection clamps
Programmable receive states	Compare high, compare low, compare three-state, compare off	Three-state: a signal level between receive high and receive low thresholds
Programmable voltage setting	Per channel	
Drive/receive voltage range	–1.5 V to +6.5 V[1] (16-bit with 152 µV resolution)	VIH − VIL ≥ 100 mV VIL (–1.5 V to +6.4 V) VIH (–1.4 V to +6.5 V)
Drive voltage accuracy	±25 mV (VIH & VIL) DUT centric (spec)	DUT centric. Maximum accuracy from ±5 °C of AutoCorrection
Receive voltage accuracy	±20 mV (VOH & VOL) DUT centric (spec)	DUT centric. Hysteresis off. Maximum accuracy from ±5 °C of AutoCorrections
Channel output short circuit current limit	±75 mA, nominal	Maximum of 250 mA per module in combination with other channels
Minimum detectable voltage swing, receive	40 mV	Nominal. Hysteresis off
Channel power-on state	high-Z	
Receive hysteresis settings	0 mV, 50 mV, 100 mV	
Channel jitter	<25 ps RMS	Typical. EPR[2] = 1 ns
Channel to channel jitter	<25 ps RMS	Typical. EPR[1] = 1 ns
Channel rise time		
@1 V pp @3 V pp @6 V pp	<450 ps <700 ps <1250 ps	At module connector into 50 Ω, 20-80%, typical
Channel fall time		
@1 V pp @3 V pp @6 V pp	<450 ps <700 ps <1250 ps	At module connector into 50 Ω, 20-80%, typical
High impedance current leakage		
Receive-only channel Receive-only, low leakage mode Bi-directional channel	±6 nA ±1.5 nA (spec) ±2 µA	Typical. Static or dynamic digital mode Dynamic digital mode only[3] Typical. Static or dynamic digital mode

[1] Drive voltage range applies to open circuit. Voltage range will be ½ stated range if driving a 50 Ω load
[2] EPR = Edge Placement Resolution
[3] The following conditions apply: 0 °C - 30 °C operating range, ±2 °C of measure leakage current, 250 mV of measure leakage voltage (±1 V range)

Data Channel Characteristics, cont.

Characteristic	Value	Comments
Active termination range	–1.5 V to +6.5 V (16-bit with 152 µV resolution)	50 Ω terminated into VIT
Active termination accuracy	±25 mV (VIT) (spec)	Maximum accuracy from ±5 °C of AutoCorrections
Active load range (IOH & IOL)	0 mA to 25 mA	Maximum of 250 mA per module in combination with
Active load accuracy	±0.40 mA (IOH & IOL)	Characteristic accuracy from ±5 °C of AutoCorrections
Commutation voltage range	–1.5 V to +6.5 V	| IOL & IOH | ≤ 1 mA
Commutation voltage accuracy	±20 mV (VCOM)	Characteristic accuracy from ±5 °C of AutoCorrections
Reflection clamp range	–2 V to +7 V (16-bit with 152 µV resolution)	VCH − VCL > 0.8 V VCL (–2 V to +6.2 V) VCH (–1.2 V to +7 V)
Reflection clamp accuracy (VCH & VCL)		
@ 1 mA @ 10 mA @ 25 mA	±30 mV ±200 mV ±400 mV	50 Ω source impedance into clamps. Characteristic accuracy from ±5 °C of AutoCorrections neglecting source impedance voltage drop

High Voltage Channel Characteristics

Characteristic	Value	Comments
Number of high voltage channels	4	
Channel control	Shared with dependent data channel	HV20 shared with CH 02 HV21 shared with CH 06 HV23 shared with CH 10 HV24 shared with CH 14
Channel impedance	<10 Ω (when forcing to terminate) 50 Ω (when forcing High or Low)	Nominal
Channel power-on state	Passive 50 Ω termination	
Maximum data rate	10 MHz	
Programmable voltage range setting	Per channel	
HV drive range	0 V to +13.5 V (16-bit with 305 µV resolution)	Force terminate
HV drive accuracy	±40 mV (VHH) (spec)	Maximum accuracy from ±5 °C of AutoCorrections
Drive voltage range	–0.1 V to +6.5 V (16-bit with 152 µV resolution)	Force high or low
Drive voltage accuracy	±35 mV (VIH & VIL) (spec)	Maximum accuracy from ±5 °C of AutoCorrections
HV drive settling time	< 4 µs @ 13.5 V pp into 1 M Ω (1nF) < 350 µs @ 13.5 V pp into 1 M Ω (1nF)	Settled to 1% of final value Typical
HV channel short circuit current limit	±60 mA, nominal	Maximum of 250 mA per module in combination with other channels. Nominal

High Voltage Channel Characteristics, cont.

Characteristic	Value	Comments
Drive source/sink current per channel	±60 mA, nominal	Maximum of 250 mA per module in combination with other channels
Drive rise time		
@ 1 V pp @ 3 V pp @ 6 V pp	<9 ps <10 ps <11 ps	Into 50 Ω, 20-80%, Typical
Drive fall time		
@ 1 V pp @ 3 V pp @ 6 V pp	<9 ps <10 ps <11 ps	Into 50 Ω, 20-80%, Typical

Open Drain Channel Characteristics

Characteristic	Value	Comments
Number of open drain channels	4	
Channel type	Output only, single-ended, ground referenced	
Channel termination	Open drain	Internal 10k Ω pull-up to +5 V
Sink current per channel	1 A max	Nominal
Channel power-on state	Off	10k Ω pull-up to +5 V
Maximum working voltage	+ 12 Vdc	

GP-IO Characteristics

Characteristic	Value	Comments
Number of GP-IO channels	2	Trigger In/Marker Out (GPIO 1/2 SMB)
Channel type	Single ended, ground referenced	
Direction control	Per channel	
Channel input impedance	50 Ω or 10 kΩ	Software selectable, DC coupled
Programmable polarity	Positive or negative slope	
Programmable threshold setting	Per channel	
Input voltage range	–2 to + 5 V	
Programmable input threshold	–2 to + 5 V	
Input threshold accuracy	±100 mV	10 kΩ input impedance
Input minimum pulse width	16 ns	
Input rate	DC to 30 MHz	
Channel output impedance	50 Ω	Marker
Output voltage	3.3 V max (into high-Z) 1.65 V max (into 50 Ω)	Nominal
Output rate	DC to 100 MHz	
Output rise / fall time	<3 ns	Typical into 50 Ω, 20%-80%
Source/sink current per channel	± 64 mA	Nominal

PPMU Characteristics

General Characteristics	Value	Comments
Number of PPMU channels	16	
PPMU modes	Force V measure V, Force V measure I, Force I measure I, Force I measure V, Force nothing, measure V	
Measurement averaging modes	None, 64 averages, 50 Hz one PLC, 60 Hz one PLC	
Measurement setup time	1 ms	Time to first measurement
Measurement speed	250 µs per channel	After setup time
Channel leakage	±10 nA	Typical
Remote sense	16 channels 1 GND	Ground sense should be tied to ground at measurement location for maximum accuracy
Remote sense leakage	±4 nA	Typical

Force/Measure Voltage	Value	Comments
Force voltage accuracy	±10 mV (spec)	Maximum accuracy from ±5 °C of AutoCorrections. Ground sense tied to ground
Measure voltage accuracy	±10 mV (spec)	With remote sense. Maximum accuracy from ±5 °C of AutoCorrections with one PLC averaging at sense location. Ground sense tied to ground
Force voltage stability	Stable at all ranges into 1 µF	Larger load capacitance possible, but response limited by current slew rate
Force voltage range		
| Current | ≤ 4 mA | Current | ≤ 25 mA | Current | ≤ 40 mA	–2 V to +6.5 V –2 V to +6 V –2 V to +5.75 V	152 µV resolution
Force voltage settling time		
40 and 1 mA ranges 100 µA range 10 µA range 2 µA range	< 20 µS < 25 µS < 100 µS < 525 µS	1 V rising and falling step settled to 1% of final value into 1 MΩ/ 1nF load. Typical

Force/Measure Current	Value	Comments
Force current accuracy	±1% of range (spec)	Maximum accuracy from ±5 °C of AutoCorrections. Remote sense disconnected.
Measure current accuracy	±1% of range (spec)	Maximum accuracy from ±5 °C of AutoCorrections with one PLC averaging. Remote sense disconnected.
Force current settling time	Dependent on load	
Force current voltage clamp range	–2 V to +6.5 V (16-bit with 152 µV resolution)	VCH > VCL VCL (–2 V to +4 V) VCH (0 V to +6.5 V)
Force current voltage clamp accuracy	±50 mV	Characteristic accuracy from ±5 °C of AutoCorrections

PPMU Characteristics, cont.

Current range and resolution		
–40 mA to + 40 mA –1 mA to + 1 mA –100 µA to + 100 µA –10 µA to + 10 µA –2 µA to + 2 µA	2.44 µA 61 nA 6.1 nA 610 pA 122 pA	Maximum of 250 mA per module in combination with other channels

Timing and Trigger Characteristics

Channel Clock	Value	Comments
Number of independent clock domains	1 - when configured as a single, 16-channel site 4 - when configured as four, 4-channel sites	Number of independent clocks depends on the number of sites selected and option
Maximum RZ clock rate on a data channel	250 MHz (option dependent)	
Minimum RZ clock rate on a data channel	5 mHz	
Clock jitter	<25 ps RMS	

Internal Reference Clock	Value	Comments
Frequency	100 MHz	
Accuracy	±25 ppm	
Period jitter	<2 ps RMS	
Reference clock sources	PXI_CLK100, PXIe-DSTARA, CLK IN	

External reference clock input (SMB front panel)	Value	Comments
Input frequency	10 MHz or 100 MHz	
Input impedance (CLK IN)	50 Ω	Nominal, AC coupled
Input voltage range (CLK IN)	+1.8 V to + 3.3 V	
Lock range accuracy	±25 ppm	
Duty cycle	40 to 60%	

Channel timing (per channel)	Value	Comments
Edge placement resolution (EPR)	1 ns minimum	Edge Placement Resolution (EPR) is specified at the time of test activation and applies to all channels within a test
Edge placement accuracy	±300 ps	
Minimum edge separation	1 EPR	
Drive edges per waveform period	2	
Receive edges per waveform period	1	
Channel-to-channel skew	±300 ps	Typical, at 1ns EPR
Minimum match loop length	4 vectors	16 ns at 1 ns EPR
Match loop latency	38 ns	

Stimulus Delay	Value	Comments
Stimulus delay range per test	254 x EPR	Can vary by channel
Stimulus delay resolution per test		
EPR ≥ 1 ns and ≤ 1.3 ns EPR > 1.3 ns	24 ps EPR	Stimulus delay adjustment with 24 ps resolution only available for EPR ≤ 1.3 ns

Response Delay Compenstation	Value	Comments
Response delay compensation range per test	254 x EPR	Can vary by channel
Response delay compensation resolution per test		
EPR ≥ 1 ns and ≤ 1.3 ns EPR > 1.3 ns	24 ps EPR	Response delay adjustment with 24 ps resolution only available for EPR ≤ 1.3 ns

Waveform characteristics		
Number of waveform tables	32	Each waveform table defines waveform characters and timing for a particular waveform period
Waveform timing change	Per vector	Each vector can utilize a different waveform table
Number of waveform characters	15	User definable
Waveform formats	RZ, RNZ, Return to tri-state, Return to active load/termination	
Generation waveform iteration count	Once, n times, infinite	
Receive post trigger sampling	0 to full record waveform	
Waveform period range		
With option SR1	EPR ≤ 2 ns: 8 x EPR to 248 x EPR EPR > 2 ns: 4 x EPR to 252 x EPR	EPR ≤ 2 ns: Waveform period must be an integer multiple of 8 times the EPR EPR > 2 ns: Waveform period must be an integer multiple of 4 times the EPR
With option SR2	4 x EPR to 252 x EPR	Waveform period must be an integer multiple of 4 times the EPR

Trigger/marker characteristics	
Trigger sources	Software Hardware: GPIO1/2, PXI_TRIG0-7, PXI_STAR, and PXIe_DSTARB
Trigger jitter	100 ns
Marker destinations	GPIO1/2, PXI_TRIG0-7, PXI_STAR, and PXIe_DSTARC

Module Calibration

Both adjustment and performance verification is required to calibrate M9195B modules. Self-maintainers can perform these procedures by using software available from Keysight:

- N7800A Test management environment
- N7876A PXI digital IO calibration application

Module adjustment requires the Y1252A adjustment cable. This accessory consists of three cable assemblies necessary for voltage and current adjustments of the M9195B. These cables are used with a high-end digital multimeter (DMM) to adjust on-board analog-digital conversion. The N7876A is required to make adjustments using this cable.

Environmental Characteristics[1,2]

Operating and Storage Conditions	Operating	Storage
Temperature[3]	0˚C to 45˚C	-40˚C to +70˚C
Altitude	3000 m	Up to 4600 m
Humidity	Type-tested at 95%, +40˚C (non-condensing)	
Calibration		
Calibration interval	1 year (Return to Keysight service center or use Y1252A with N7800A/N7867A)	
Warm-up time	30 minutes	
Vibration		
Operating random vibration: type-tested at 5 to 500 Hz, 0.21 g rms		
Survival random vibration: type-tested at 5 to 500 Hz, 2.09 g rms		

Regulatory Characteristics

Safety
Complies with the essential requirements of the European Low Voltage Directive as well as the current versions of the following standards (dates and editions are cited in the Declaration of Conformity): – IEC/EN 61010-1 – Canada: CSA C22.2 No. 61010-1 – USA: UL std no. 61010-1
EMC
Complies with the essential requirements of the European EMC Directive as well as the current editions of the following standards (dates and editions are cited in the Declaration of Conformity): – IEC/EN 61326-1 – CISPR Pub 11 Group 1, class A – AS/NZS CISPR 11 – ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conformea la norme NMB-001 du Canada
South Korean Class A EMC declaration
Information to the user: This equipment has been conformity assessed for use in business environments. In a residential environment this equipment may cause radio interference. – This EMC statement applies to the equipment only for use in business environment.
사 용 자 안 내 문
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[1] Samples of this product have been type tested in accordance with the Keysight Environmental Test Manual and verified to be robust against the environ- mental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions.

[2] Test methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3

[3] De-rate max temperature by 5°C above 2000 m.

Ordering Information

Software

Supported Software Components	
Operating systems	Microsoft Windows 7 and 10 (64-bit only)
Standard compliant drivers	IVI-COM, IVI-C, MATLAB, and LabVIEW
Application development environments (ADE)	LabVIEW, MATLAB, Visual Studio.NET (C/C++, C#, VB.NET), Command Expert
Keysight IO libraries	Version 2018 update 1 (or greater)
Development Software	
M9192A	DSR pattern editor software
M9193A	DSR pattern editor with data conversion software

Hardware

Model	Description
M9195B	PXIe Digital Stimulus/Response with PPMU: 250 MHz, 16 Ch
M9195B-M01/M06/M12	Memory, 16/64/125 Mvectors/ch
M9195B-S01/S04	Single site/multi-site enabled
M9195B-SR1/SR2	Max clock rate, 125 MHz/250 MHz
M9195B-MMS	Multi-module sync
Accessories	
Y1245A, Y1246A, and Y1247A	Single-site DSR cable: 0.5, 1.0, or 2.0m
Y1248A or Y1249A	Multi-site DSR cable: 1.0, or 2.0m
Y1250A or Y1251A	Module sync cable: four or twelve modules
Y1252A	DSR adjustment cable
Y1253A	DSR Evaluation and prototyping board
Y1254A or Y1255A	DSR SMA breakout cable: 1 or 2m

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