DATA SHEET

# M9032A and M9033A

## System Synchronization Modules

## Introduction

The M9032A and M9033A are high-performance System Synchronization Modules used to synchronize multiple modules across multiple chassis.


KEYSIGHT TECHNOLOGIES

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## Description

The M9032A/M9033A PXIe System Synchronization Module (SSM) provides multi-module/multi-chassis synchronization and triggering for Keysight's modular systems, as well as other Keysight instruments. It meets the STM specifications documented in the PXI Express Hardware Specification.

The M9032A is a single slot and the M9033A is a double slot 3U PXIe module that is compatible with Keysight's PXIe chassis. It includes a high-quality Oven Controlled Crystal Oscillator (OCXO) reference clock, flexible signal connections between front panel and backplane trigger resources, and accurate phase measurement capability on select clock paths, in order to achieve a very tight synchronization among various measurement products.

The M9032A/M9033A modules use the newly defined System Sync standard to distribute reference clock, low-latency LVDS triggers, and high bandwidth/speed information through Multi-Gigabit Transceiver (MGT) links across multiple instruments. The System Sync connector provides a forward and reverse clock link to facilitate cable delay measurement and compensation, up to 12 LVDS pairs for low latency trigger or data transition, and another 4 MGT pairs (TX and RX) for higher bandwidth data transfer, up to 5 Gbps.

These modules can also support time synchronization to common time standards delivered through various options. These options enable these modules to synchronize measurement systems to actual Time of Day marks, allowing for precisely time-stamped measurement data from spatially dispersed equipment to be correlated.

The M9032A/M9033A modules include a Virtex UltraScale Plus FPGA to support enhanced features in the future versions of the software.

## Key Features

- Two form factors: single and double PXIe slot
- PathWave Test Sync Executive support
- Virtex UltraScale+ VU3P FPGA with PathWave

# M9032A and M9033A Hardware Overview

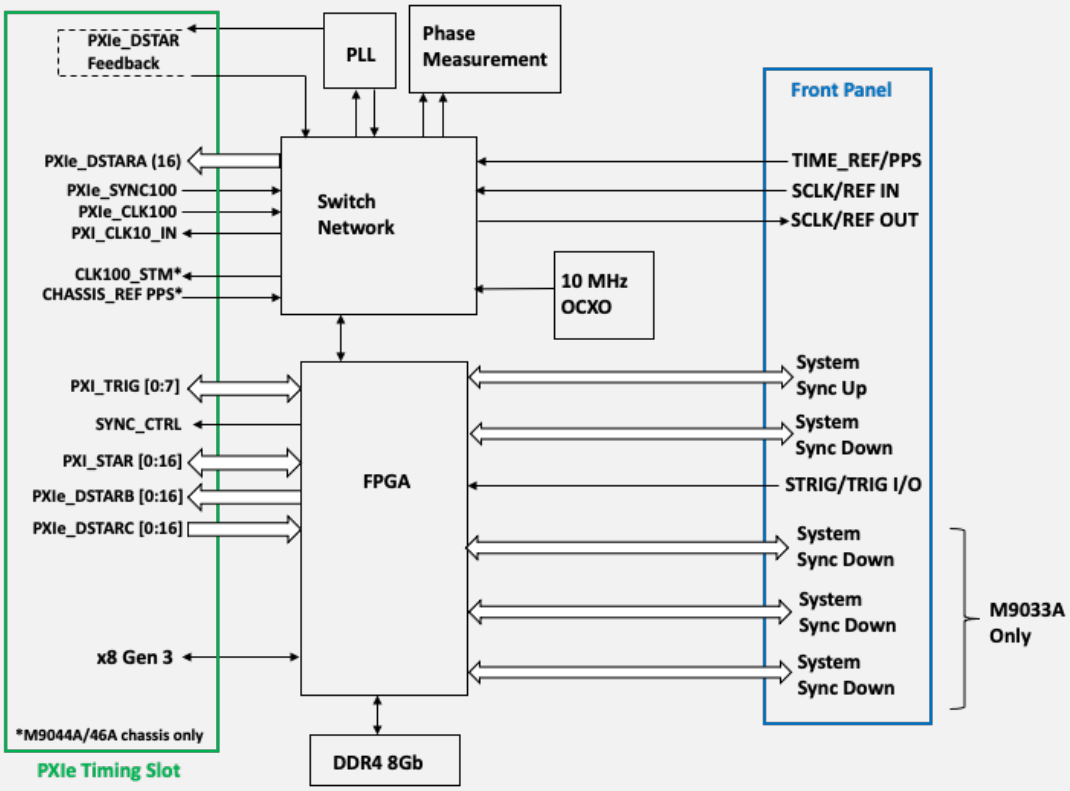


Figure 1. M9032A and M9033A Block Diagram

## Front panel

The M9032A and M9033A front panels have 4 SMP male connectors: External Reference Clock output, programmable trigger input/output, time reference or PPS input, and External Reference Clock input. The M9032A features one System Sync Upstream and one System Sync Downstream connector, and the M9033A features one System Sync Upstream and four System Sync Downstream connectors.

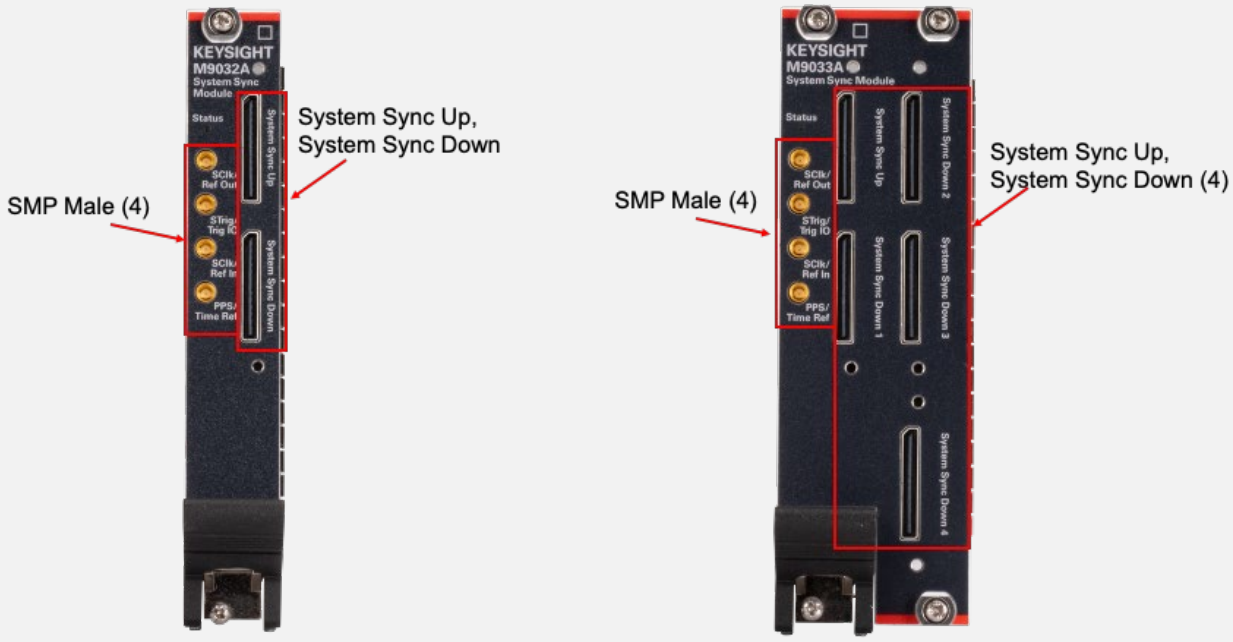


Figure 2. M9032A and M9033A Front Panel

# M9032A and M9033A Software Overview

## PathWave Test Sync Executive

The PathWave Test Sync Executive enables rapid development of high performance, multi-channel, real-time synchronous solutions. It is enabled on the M9032A and M9033A with option HV2 and has seamless interaction with PathWave FPGA (option PWP). The Sync Executive features:

- Transparent multi-module synchronization by precisely time aligning multiple channels in the same module or across several modules
- Real-time synchronous execution including sequencing, branching, and looping
- Time-deterministic hardware-based execution

## PathWave FPGA

PathWave FPGA is a system-level FPGA development environment which enables you to open and customize the M9032A and M9033A. When combined with option PWP, you now have access to the user-programmable FPGA and can insert your custom logic into the instrument. You can begin from HDL or a design in the included library and add or import Vivado and MATLAB components. Key benefits:

- Process signals in real time or accelerate bottleneck operations by running as hardware-in-the-loop
- Achieve your test requirements by inserting your own IP into the instrument
- Scale-up designs or channel counts by adding multiple M9032A or M9033A

## Soft front panel

The soft front panel (SFP) provides a graphical user interface that allows the user to set up the most used functionality of the system synchronization module. The SFP also gives the user the ability to check the module's connection status, configure the reference clock and IO settings, and perform frimware updates.

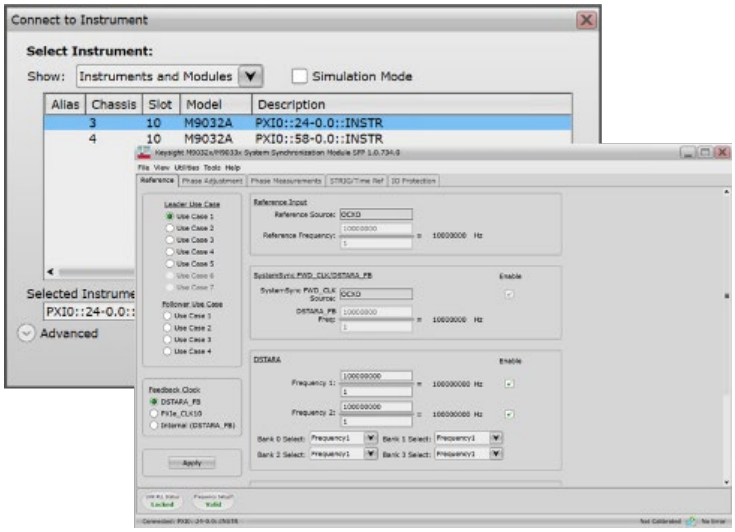


Figure 3. M9032A and M9033A Soft Front Panel

# Technical Specifications

| General characteristics[1] | | |
|---|---|---|
| **Module characteristics** | | |
| Bus interface and compatibility | | PXIe peripheral module (x8 Gen3) |
| Volatile module memory | | 1 GB (DDR4) |
| | **M9032A** | **M9033A** |
| Chassis requirements | One 3U PXI Express slot | Two 3U PXI Express slots |
| Front panel connectors | Four SMP male, 50 Ω | Four SMP male, 50 Ω |
| | Two OCuLink, 85 Ω | Five OCuLink, 85 Ω |
| Front panel indicator | 1 tricolor LED | 1 tricolor LED |
| Size | 3U/1-slot PXI/CompactPCI standard 21.8 x 130.8 x 209.2 mm[2] (W x H x D) | 3U/2-slot PXI/CompactPCI standard 42.2 x 130.8 x 209.2 mm[2] (W x H x D) |
| Weight | 0.45 kg (1.0 lbs) | 0.74 kg (1.6 lbs) |

| Power requirements | | |
|---|---|---|
| **Backplane supply** | **M9032A (single slot)** | **M9033A (dual slot)** |
| | **Typical** | **Typical** |
| +12 V | 3.10 A, 5.04 A[3] | 3.20 A, 6.48 A[3] |
| +3.3 V | 2.95 A | 2.95 A |
| +5 VAUX | 6 mA | 6 mA |

| Clocks and trigger characteristics | |
|---|---|
| **SCLK/Ref In input** | |
| Input coupling | AC |
| Input impedance | 50 Ω |
| Minimum input swing with 50% duty cycle | 400 mVpp |
| Maximum input swing with 50% duty cycle | 2.4 Vpp |
| Frequency range | 1 MHz to 150 MHz[4] |
| **STRIG/TRIG IO input** | |
| Input coupling | DC |
| Input termination | 2kΩ to 2.64 V |

[1] All characteristics are typical and intended to provide additional information including the expected performance of an average unit that is not covered by the product warranty. Performance of a customer unit to typical specifications may or may not be measured during a calibration service.

[2] Includes connectors and handle extensions

[3] Refers to typical usage with PathWave FPGA Sandbox and System Sync 5V output at 1 A per port. PathWave FPGA usage requires high power chassis.

[4] Supported frequencies based on frequency planner

| | |
|---|---|
| Input threshold | Adjustable, 100 mV to 3.2 V, ±100 mV |
| Input voltage range | 0 - 3.3 V |
| **PPS/Time Ref input** | |
| Input coupling | DC |
| Input termination | 2.5 kΩ to 3.3 V |
| Input threshold | Adjustable, 100 mV to 3.2 V, ±100 mV |
| Input voltage range | 0 - 3.3 V |
| **SCLK/Ref Out output** | |
| Output coupling | AC |
| Expected termination | 50 Ω |
| Typical Amplitude | 800 mVpp |
| Frequency range | 1 MHz to 150 MHz[4] |
| Rising/falling edge (20%, 80%) | 220 ps, typical |
| Duty cycle | 45% to 55% |
| **STRIG/TRIG IO output** | |
| Output coupling | DC |
| Expected termination | 50 Ω or high impedance |
| Typical Amplitude | 1.7 Vpp into 50 Ω, 3.3 Vpp into high impedance |
| Rising/falling edge into 50 Ω load (20%, 80%) | 980 ps, typical |
| **OCXO** | |
| Nominal frequency | 10 MHz |
| Stability | ±1.0 ppm |
| **PXIe DSTARA LVPECL signal[5]** | |
| Voltage high output | 2.328 V, typical |
| Voltage low output | 1.550 V, typical |
| Maximum frequency | 150 MHz |
| **PXIe DSTARB LVDS signal** | |
| Differential output voltage | 350 mV, typical |
| Output common-mode voltage | 1.250 V, typical |
| **PXIe DSTARC LVDS signal** | |
| Differential input voltage | 350 mV, typical |
| Input common-mode voltage (DC coupling) | 1.200 mV, typical |
| **PXI trigger** | |
| I/O voltage level | 3.3 V LVCMOS I/O, 5 V input tolerance |
| **PXI star** | |
| I/O voltage level | 3.3 V LVCMOS I/O, 5 V input tolerance |

[5] Loaded with 50 Ω to 1.3 V or Thevenin equivalent for proper operation

| Environmental characteristics[6] | | |
|---|---|---|
| **Operating and storage conditions** | | |
| Temperature | Operating:<br>0 °C to 45 °C | Storage:<br>-40 °C to 70 °C |
| Altitude | Operating:<br>Up to 10,000 ft (3048 m) | Storage:<br>Up to 15,000 ft (4572 m) |
| Maximum relative humidity | Type tested, 95%RH up to 40 °C, decreases linearly to 40% RH at 45 °C | |
| Pollution degree | Pollution degree 2[7] | |

| Regulatory characteristics |
|---|
| **Safety** |
| Complies with the current versions of the following standards:<br>- IEC/EN 61010-1, 3rd Edition<br>- Canada: CSA C22.2 No. 61010-1-12<br>- USA: UL std no. 61010-1, 3rd Edition |
| **EMC** |
| Complies with European EMC Directive 2004/108/EC as well as the current editions of the following standards:<br>- AS/NZS CISPR 11<br>- IEC/EN 61326-1<br>- ICES/NMB-001<br>- CISPR Pub 11 Group 1, Class A<br>This ISM device complies with Canadian ICES-001.<br>Cet appareil ISM est conforme a la norme NMB-001 du Canada. |

[6] This instrument is intended for indoor use only

[7] Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.

# Ordering Information

## Software

| Supported software components | |
|---|---|
| Supported operating systems (pre-installed) | Windows 10 |
| Standard compliant drivers | IVI.NET (64-bit) |
| Application development environments | Python version 3.7, Visual C++ |
| Keysight IO libraries suite (Pre-installed) | Keysight IO libraries suite 2022 (version 18.2.27313.1) |

## Hardware

| Model | Description |
|---|---|
| M9032A | PXIe System Synchronization Module, 2 port |
| M9033A | PXIe System Synchronization Module, 5 port |
| **Accessories** | |
| Y1320A | System sync/link cable, x4-x4, 0.5 m |
| Y1321A | System sync/link cable, x4-x4, 1.0 m |
| Y1323A | System sync/link cable, x8-2, x4, 0.5 m |
| Y1324A | System sync/link cable, x8-2, x4, 1.0 m |
| Y1326A | System sync/link cable, x8-x8, 0.5 m |
| Y1327A | System sync/link cable, x8-x8, 1.0 m |
| Y1329A | System sync/link cable, x8-x8, 2.0 m |
| Y1330A | MCX(m) to MCX(m) cable, phase stable, 0.3 m |
| Y1331A | MCX(m) to MCX(m) cable, phase stable, 1.0 m |
| Y1332A | MCX(m) to MCX(m) cable, phase stable, 2.0 m |
| Y1333A | SMA(m)-SMP(f) cable, 0.3 m |
| **Related products** | |
| M9018B and M9019A | 18-slot PXIe chassis, Gen 2 or Gen 3 |
| M9010A | 10-slot PXIe chassis, Gen 3 |

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