DATA SHEET

M8050A
High-performance BERT 120 GBd
Internal version 2.5

New features: Adjustable ISI, segmented SSC for USB4.x, BUJ with additional filters for 800G, accelerated error analysis with UXR

Enabling Your Successful Design Deployments in 800G/1.6T

The Keysight M8050A BERT enables success in chip deployments of 800G/1.6T and other leading technologies by providing an unmatched combination of 120 GBd signaling with uncompromised signal integrity.

KEYSIGHT TECHNOLOGIES

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Introduction

The Keysight M8050A high-performance BERT enables accurate characterization of receivers used in next generation data center networks and server interfaces with symbol rates up to 120 GBd.

The M8050A high-performance BERT is one part of the Keysight M8000 Series of BER test solutions. It can be combined with other hardware and software of the M8000 Series.

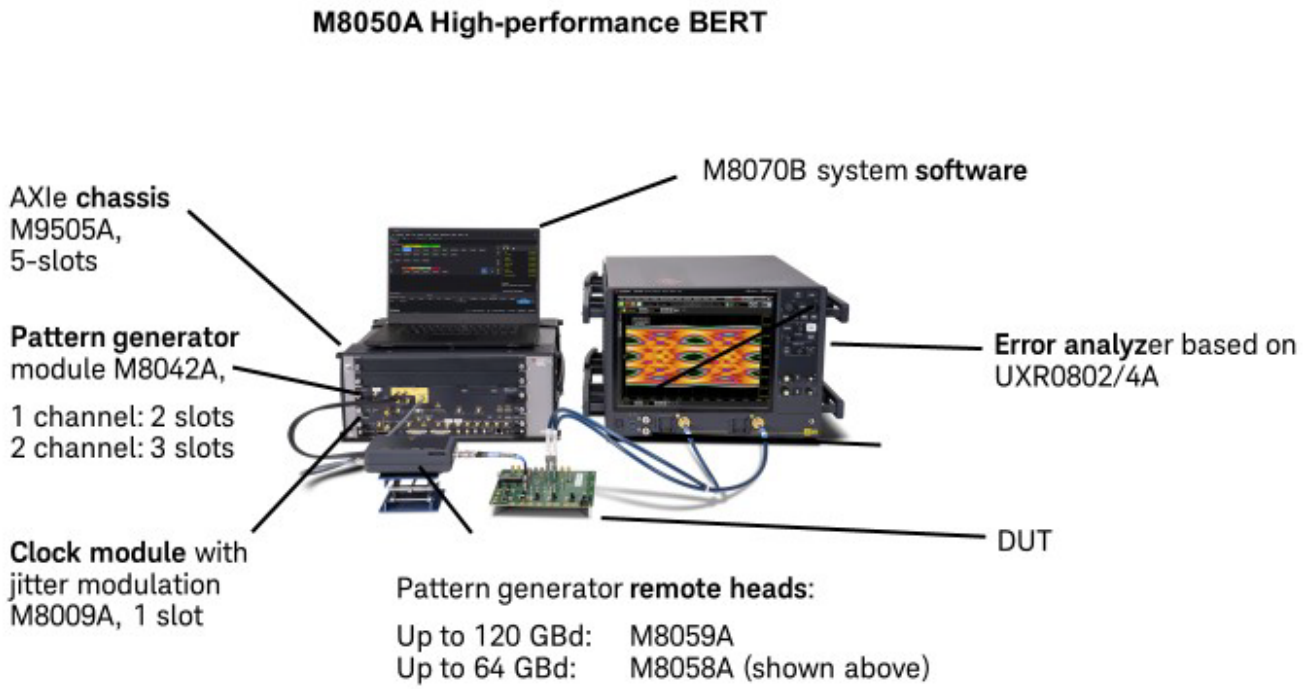

Figure 1. Overview of the M8050A high-performance BERT

Overview of M8050A modules and remote heads covered in this data sheet:

Description	AXIe slots	Product number
120 GBd pattern generator module for one data output channel	2-slot	M8042A-0G1
120 GBd pattern generator module for two data output channels	3-slot	M8042A-0G2
64 GBd remote head with cable connections to M8042A pattern generator module		M8058A
120 GBd remote head with cable connection to M8042A pattern generator module		M8059A

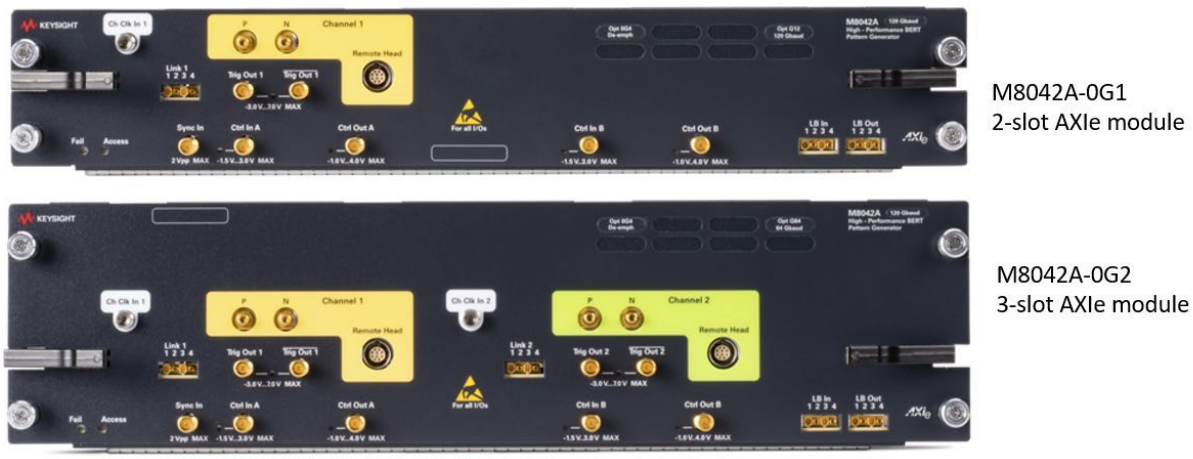

Figure 2. The pattern generator module M8042A is available as one channel and two channel version. The one channel version M8042A-0G1 occupies 2 slots in the AXIe chassis, the two-channel version M8042A-0G2 occupies 3 slots.

Pattern generator remote head up to 120 GBd
M8059A

Pattern generator remote head up to 64 GBd
M8058A

Figure 3. Two remote heads are available for the pattern generator module M8042A. At the left side the 120 Gbd remote head M8059A is shown with its 1.0 mm connectors to accommodate close connection to the device under test for symbol rates up to 120 GBd. The 64 GBd remote head M8058A is shown at the right side and this provides 1.85 mm connectors. The three cables on the back side of the remote heads are used to connect with the M8042A pattern generator module and are not removable.

The M8042A pattern generator module operates from 2 to 120 GBd. It is available as one channel or two channel version. You can select three symbol rate ranges. The M8042A requires the clock module with jitter modulation M8009A, and one remote head for each data output channel. For operation above 64 GBd the 120 GBd pattern generator remote head M8059A is required. Using the P and N output of the M8042A module is prohibited. One M8009A clock generator module is required for each M8042A pattern generator module.

For the following generator functions these module options are required:

- Pattern generation up to 32 GBd for NRZ and PAM4 (M8042A-G32)
- Pattern generation up to 64 GBd for NRZ and PAM4 (M8042A-G642)
- Pattern generation up to 120 GBd for NRZ and PAM4 (M8042A-G12)
- One channel (M8042A-0G1)
- Two channels (M8042A-0G2)
- De-emphasis, module-wide license (M8042A-0G4)
- PAM6 encoding for 224 Gbps interfaces (M8042A-0P6)
- PAM8 encoding for 224 Gbps interfaces (M8042A-0P8)
- Future options are tbc

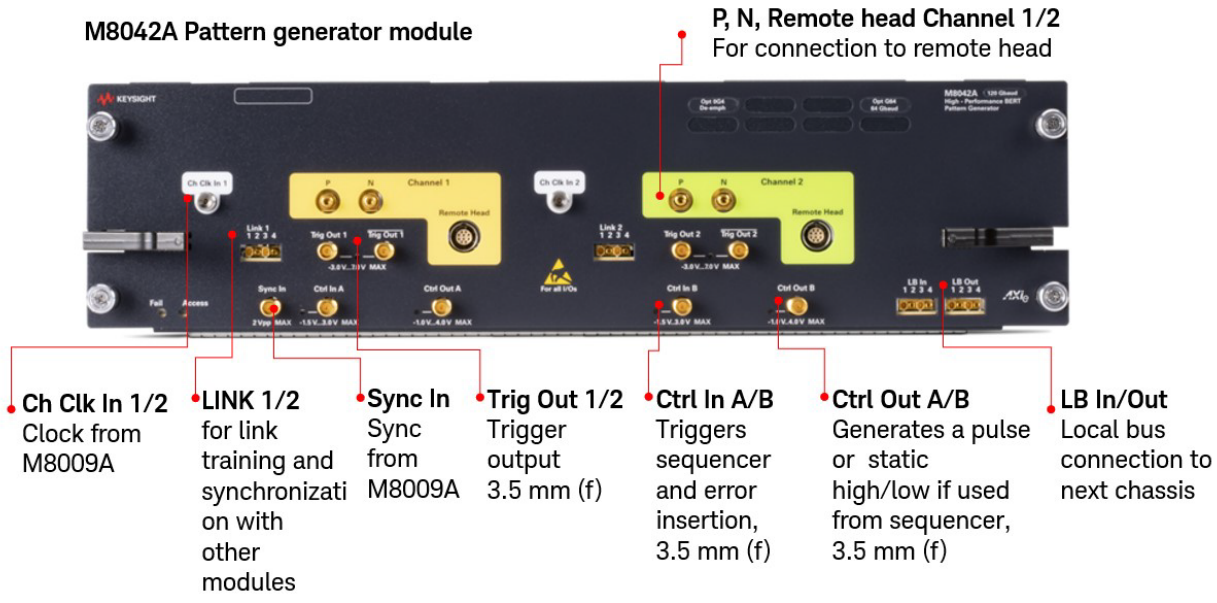

Figure 4. The M8042A pattern generator module provides many supplementary inputs and outputs. Shown here is the overview of all inputs and outputs for a two-channel version of M8042A.

Data Output (Data Out 1, Data Out 2)

Table 1. Data output characteristics for M8042A with M8058A/M8059A. Values apply at the end of the reference cable at the outputs of the remote heads M8058A, M8059A.

Parameter	with M8059A	with M8058A
Symbol rate	2.000 to 120.0 GBd for M8042A-G12 2.000 to 64.8 GBd for M8042A-G64	2.000 to 64.8 GBd for M8042A-G64 2.000 to 32.4 GBd for M8042-G32

Parameter	with M8059A	with M8058A
	2.000 to 32.4 GBd for M8042-G32 Applies for NRZ and PAM4	Applies for NRZ and PAM4
Data formats	NRZ, PAM4. PAM6 (requires M8042A-0P6/UP6). The maximum supported symbol rate is 96 GBd, over-programming is possible. PAM8 (requires M8042A-0P8/UP8). The maximum supported symbol rate is 80 GBd, over-programming is possible.	
Channels per module	channel, 2 slots (option 0G1) channel, 3 slots (option 0G2)	
Amplitude	100 mVpp to 1.6 Vpp differential 50 mVpp to 0.8 Vpp single ended	100 mVpp to 1.8 Vpp differential 50 mVpp to 0.9 Vpp single ended
Amplitude resolution	1 mV	
Symbol level resolution	PAM4 levels are adjustable in 0.5% steps of amplitude	
Amplitude accuracy	±10% ±10 mV typical (AC) [1]	
Output voltage window	–1 to +3.0 V depends on external termination voltage [2]	
Common mode voltage accuracy	25 mV +- 12.5% [5]	
External termination voltage	–1 to +3.0 V	
Termination modes	Balanced and unbalanced	
Termination impedance range	Balanced 100 Ω ±30 Ω Unbalanced 50 Ω ±15 Ω Unused outputs should be terminated with 50 Ω. Operation into open is possible but not specified	
Coupling	DC/AC selectable coupling	
Transition time (20 to 80 %)	4 ps typical (20 to 80%) at 120 GBd 6.5 ps typical (20 to 80%) at 64 GBd 8 ps typical (20 to 80%) at 8 GBd	7 ps typical (20 to 80%) at 64 GBd 8.5 ps typical (20 to 80%) at 8 GBd
Intrinsic total jitter [6]	3.3 ps typical in combination with M8009A. 7 ps typical from 70 to 80 GBd 6 ps typical from 16 to 33 GBd	

Parameter	with M8059A	with M8058A
	7 ps typical from 10 to 16 GBd 9 ps typical from 2 to 10 GBd	
Intrinsic random jitter [6] (NRZ)	10 mUI rms typical. 15 mUI rms typical from 105 to 120 GBd 20 mUI rms typical from 99 to <105 GBd 40 mUI rms typical from 70 to 80 GBd 15 mUI rms typical from 30 to 33 GBd 7 mUI rms typical from 24 to 30 GBd	
Clock/2 jitter range	±50 mUI or ±4 ps typical (whatever is less) for symbol rates above 12 GBd. Note: this means that first eye can be up to 50 mUI or 4 ps longer or shorter than subsequent eye	
Adjustable clock/2	For each channel independently	
SNDR [3]	53.125 GBd: 35 dB typical 106 GBd: 31 dB typical	53 to 58 GBd: 35 dB typical
Level random noise	53.125 GBd: 4.75 mV rms differential typical 106 GBd: 6 mV rms differential typical	53 to 58 GBd: 5.5 mV rms differential typical
Data delay	Delay range 100 ns Delay accuracy: ± (maximum (1.0 ps or 25 mUI whatever is higher) + 1% of entered value) typical	
Skew between normal and complement	2 ps maximum at the end of the reference cable pair. Fixed. 1 ps maximum at connector or M8059A Reference cable pair M8059A-801 has 1 ps	2 ps maximum at the end of the reference cable pair. Fixed. 1 ps maximum at connector or M8058A Reference cable pair M8058A-801 has 1 ps
Skew between data output ch 1 and ch 2 in one module	Within same M8042A module: Repeatability: tbd Absolute skew: tbd	
Electrical idle, (squelch)	The output transitions from full swing to 0 V amplitude and vice versa at constant offset within 1 UI. NRZ: normal and complement output have same level (Max – Min)/2 PAM4: normal and complement output have same level (Max (lev3) – Min (lev 0))/ 2.	
Squelch granularity	When controlled from sequencer: 512 UI	

Parameter	with M8059A	with M8058A
Automatic eye performance optimization by using an external oscilloscope	Yes, requires M8070ADVB.	
Connectors at data output of M8042A	1.0 mm, female	
Connectors at data output of remote head	1.0 mm, female	1.85 mm, female
Reference cables	Matched cable pair 1.0 mm (m) to 1.0mm (m), 150 mm, 1 ps M8059A-801. (Keysight part number M8059-61621)	Matched cable pair 1.85 mm (m) to 1.85 mm (m), 150 mm, 1 ps M8058A-801. (Keysight part number M8199-61610)

1. At 5 GBd measured with DCA-X N1046A and clock pattern and in the middle of the eye
2. High level voltage range= 2/3* Vterm - 0.95 V < HIL < Vterm + 2 V . Low level voltage range= 2/3 * Vterm - 1 V < LOL < Vterm + 1.95 V
3. Measurement procedure according to section 120D.3.1.6 of IEEE specification
4. Measured at 90% of maximum amplitude
5. Common mode voltage = 0.5 * (measured offset at Normal + measured offset at Complement). Measured with DCA N1046A and 10dB attenuator.
6. Measured with N1060A and PTB signal from Ref clk out 16G from M8009A, NRZ, PRBS15, @ BER 1e-12

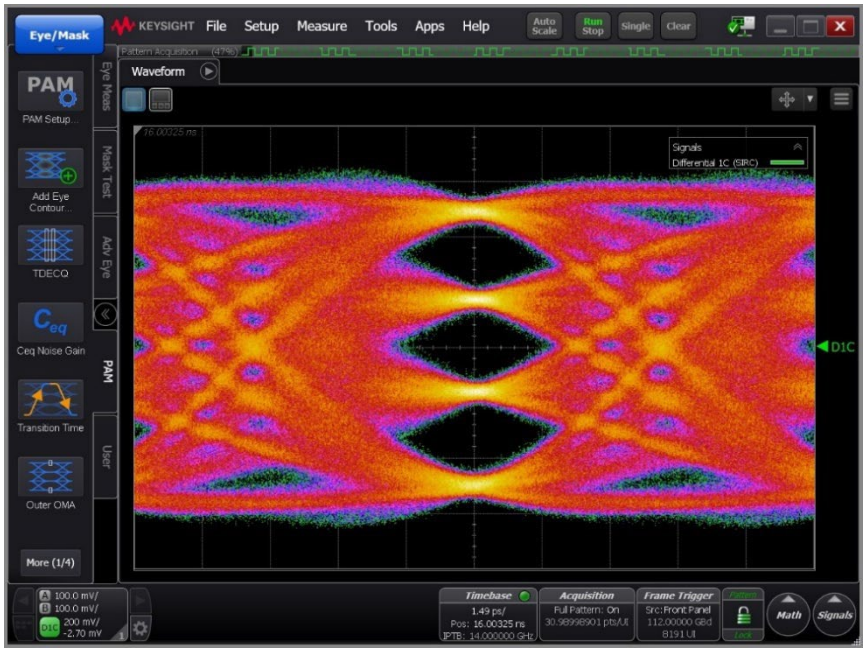

Figure 5. Clean 112 GBd PAM4 output signal of M8042A pattern generator module M8042A with remote head M8059A. This uses the clock module M8009A with internal oscillator. The output amplitude is set to 1.0 Vpp differential and PRBS 2^{15}-1. Measured with DCA-X and N1046A.

De-emphasis

The M8042A provides built-in de-emphasis with positive and negative cursors based on a finite impulse response (FIR). Users can enter the de-emphasis in coefficient values.

Table 2. De-emphasis characteristics for M8042A. Requires option -0G4

De-emphasis	Range if used as cursor	Range if used as main cursor
De-emphasis taps	7, can be adjusted for each channel independently 1 UI spacing	
Cursor (c0)	0.0 to ±0.45 [1]	
Cursor (c1)	0.0 to ±0.45 [1]	
Cursor (c2)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c3)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c4)	0.0 to ±0.45 [1]	0.3 to 1.0 [1]
Cursor (c5)	0.0 to ±0.45 1	
Cursor (c6)	0.0 to ±0.45 1	
Cursor coefficient resolution	0.004 hardware capable resolution, user interface allows 0.001 steps	
Main cursor	Configurable position between c2 and c4	

1. Sum of all cursors absolute values may not exceed 1.0. Each absolute value of a cursor must be < as value of main cursor.

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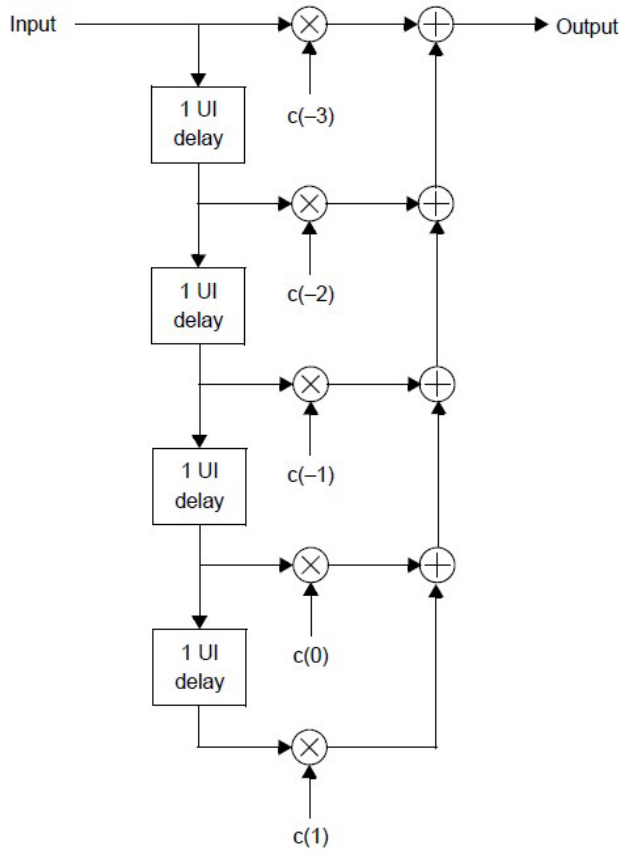

Figure 6. The pattern generator provides built-in de-emphasis to emulate a TX equalizer. The example shows a configuration for IEEE802.3 ck with three pre-cursors c(-3), c(-2) and c(-1), the main cursor c(0), and one post cursor c(1).

Trigger output 1/2 (Trig Out 1, Trig Out 2)

The trigger output can be used in different modes:

- Divided clock with dividers:
  - Max output frequency is 8.0 GHz, divider range 2 to 65000
  - For trigger output frequency ≤ 8.1 GHz: divider range n to 65000
  - Minimum divider n is the next lower integer value below the symbol rate/ 8 GHz
  - (example: for a symbol rate of 53 GBd, n = 6, because it is the next lowest integer of 53/8 = 6.625)

- Sequence block trigger and offset
  - Pulse mode triggered by sequencer (only if memory pattern is used)
  - “Pulse on PRBS” mode NRZ only. Matched pattern without ignoring defined bits (only if algorithmic pattern is used)
  - Pulse width not freely adjustable

The trigger output 2 is only available for the two-channel version of M8042A.

Table 3. Trigger output characteristics of M8042A

Parameter	
Amplitude	0.1 to 1.0 Vpp single ended
Jitter injection	The injected jitter is always the same as the jitter at the Data OUT (excluding clk/2)
Delay	Follows Data Out delay Relative Trigger to Data Out delay: Range: 0 to 1000 UI with 1 UI resolution
Skew between trigger output and data output of same channel	Tbd
Output voltage window	–1 to 3 V [1]
External termination voltage	–1 to 3 V
Interface	50 Ω
Connector	3.5 mm, female

1. High level voltage range= 2/3*Vterm – 0.95 V < HIL < Vterm + 2 V
Low level voltage range= 2/3 *Vterm – 1 V < LOL < Vterm + 1.95 V

Control input A/B (Ctrl In A, Ctrl In B)

Each control input can be selected as: sequence trigger, error insertion.

Table 4. Control input characteristics

Parameter	
Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Termination voltage accuracy	± (25 mV +1%)
Threshold voltage	–1 V to +3 V
Delay repeatability to data output	Tbd
Absolute delay to data output	< 1 ms
Connector	3.5 mm, female

Control output A/B (CTRL Out A, CTRL Out B)

This output provides a pulse or static high/low if used from sequencer

Table 5. Control output A/B characteristics

Parameter	
Amplitude [1]	0.1 to 2 V
Output voltage window [1]	–0.5 to 1.75 V
Delay to data output	Tbd
Connector	3.5 mm, female

1. When terminated with 50 Ω into GND. Doubles into open.

LINK 1/2 (Link1, Link 2)

LINK 2 is only available for the two-channel version of M8042A.

This communication link enables interactive link training with low latency between a pattern generator channel and a M8046A analyzer module. Requires cable M8051A-801.

Channel clock input 1/2 (Ch Clk In 1/2)

The channel clock inputs are used to connect with the M8009A clock module.

The channel clock input 2 is only available for the two-channel version of M8042A.

Connector: 1.85 mm, female

These are the supported cables to connect M8042A with M8009A:

- M8042A-801: Clock cable semi-rigid for M8042A channel 1 (part number M8042-61621)
- M8042A-802: Clock cable semi-rigid for M8042A channel 2 (part number M8042-61622)

Alternatively, to the semi-rigid clock cable, the 450 mm clock cable 1.85 mm (m) to 1.85mm (m) can be used (part number M8199-61624, included in M8042-810 cable kit)

Synchronization input (Sync In)

The synchronization input is used to connect with M8009A clock module.

Connector: 3.5 mm, female

This is the supported cable to connect M8042A with M8009A:

- M8042A-801: Synchronization cable, 3.5 mm, semi-rigid for M8042A and M8009A (part number M8042-61623)

Local bus input/output (LB In, LB Out)

The local bus input is needed for communication connected to the previous AXIe chassis.

The local bus output is needed for communication connected to the next AXIe chassis.

The connection cable is a 4-wire mini coax cable M8051A-801 (part number M8041-61601)

Pattern and Sequencing

Table 6. Specifications for patterns and sequencing

Parameter	
PRBS	2^n-1, n= 7, 10, 11, 15, 23, 23p, 31, 33, 35, 39, 45, 49, 51
PRBS	2^n, n=7, 10, 11, 13, 15
QPRBS	OIF-CEI: QPRBS13-CEI, QPRBS31-CEI IEEE 802.3: QPRBS13, PRBS13Q, PRBS31Q
User definable pattern memory	NRZ: 8 Mbit/ channel PAM4: 4 Msymbols/ channel PAM6 and PAM8: 4 Msymbols/ channel
Pattern	Export, import. Or factory patterns provided by M8070B
Mark density	PRBS 1/8 to 7/8
PAM4 coding	Gray coding, Uncoded, custom mapping of 00, 01,10,11 to symbols 0, 1, 2, 3.
Pre-coder	Yes (only for NRZ and PAM4)
PAM6 coding	Uncoded Custom mapping of 000, 001,010,011,100,101 to symbols 0, 1, 2, 3, 4, 5. 110 and 111 are interpreted as symbol 0. Memory based patterns only
PAM8 coding	Uncoded Custom mapping of 000, 001,010,011,100,101,110, 111 to symbols 0, 1, 2, 3, 4, 5, 6, 7.

	Memory based patterns only
Vector/ sequencer granularity	NRZ: 512 bit, PAM4/6/8: 256 Symbols
Pattern sequencer	3 counted loop levels, 1 infinite loop, # of blocks: 500 Minimum block length NRZ: 2048 Bits Minimum block length PAM4/6/8: 1024 Symbols
Squelch	For NRZ per UI
Error insertion	Single symbols, ratio variable/ fixed. Manual, CTRL IN and sequencer break

Specifications for Clock Module with Jitter Modulation M8009A

Figure 7. Clock module M8009A-061 with jitter modulation.

The M8009A clock module with integrated jitter modulation operates from 4 to 60 GHz. It can be locked to external reference clocks.

For the following functions a module option is required:

- Advanced jitter modulation for up to two channels, license (M8009A-0G3)
- Reference clock multiplier, license (M8009A-0G6)

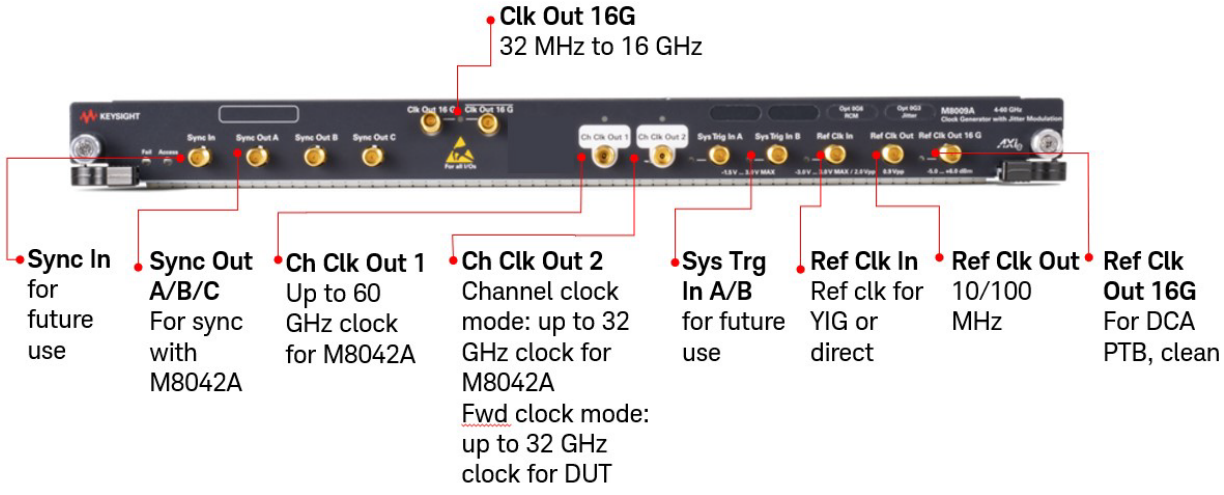

Figure 8. This figure gives an overview of all inputs and outputs of the M8009A-061 clock module with jitter modulation

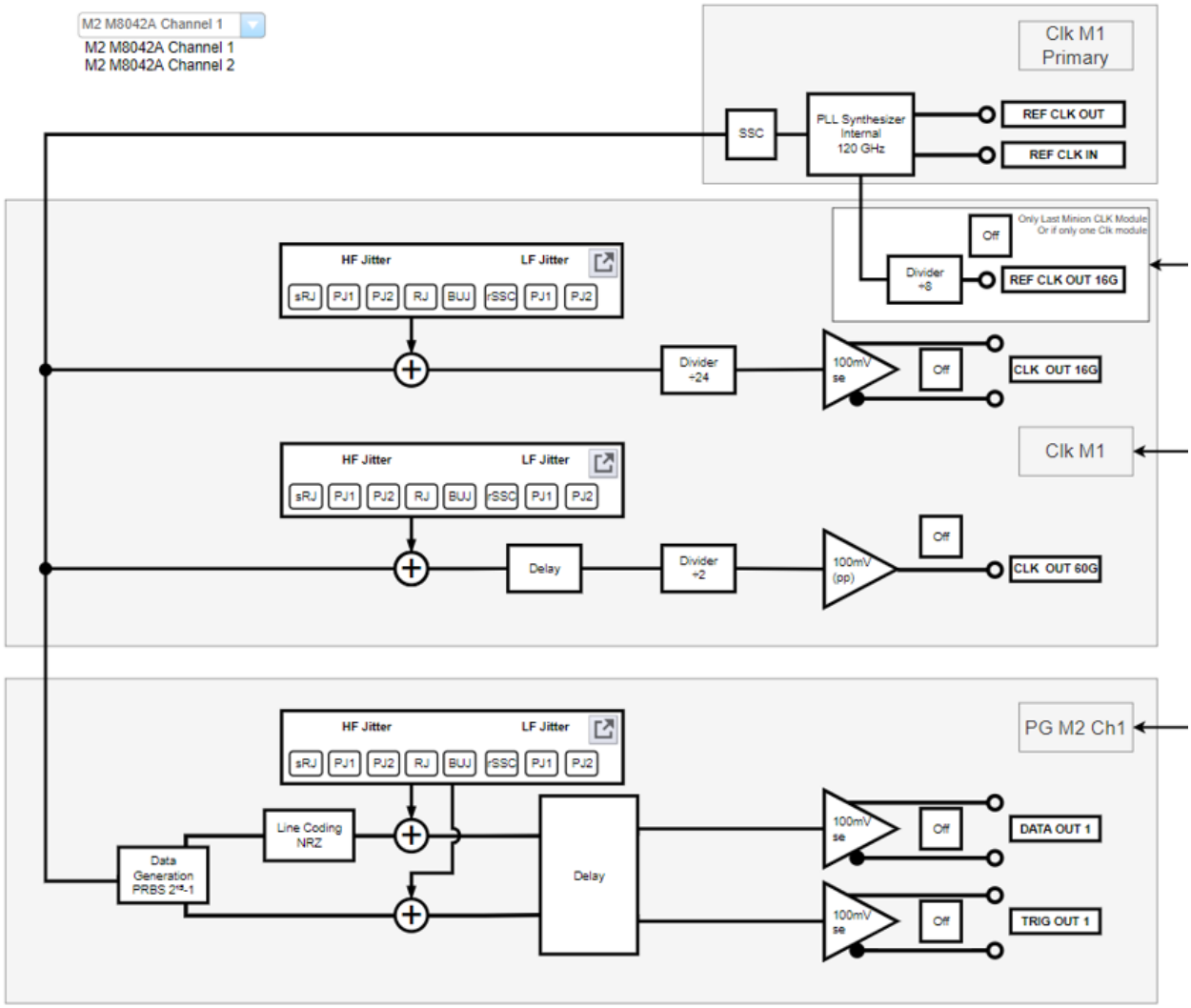

Figure 9. Simplified block diagram of M8009A-061 clock module with jitter modulation and M8042A pattern generator module. Shown is a one channel configuration.

Internal Synthesizer and Clock Modes for M8009A

Table 7. Internal synthesizer characteristics of M8009A

Parameter	
Frequency accuracy	±2 ppm
Frequency resolution	1 Hz

Table 8. Clock modes for M8009A

Clock mode	Clock generation	Input frequency range
Internal	PLL with internal reference	N/A
Reference clock	PLL with bandwidth < 100 kHz	10 or 100 MHz
Direct clock	No PLL. Maximum output frequency is 60 GHz	8 to 16.2 GHz
Reference clock with multiplier bandwidth	Multiplying PLL with m/n PLL with loop bandwidth: 100 kHz, others: see table 12, m, n = 1 to 12000	10 MHz to 16.2 GHz

Channel clock output 1 (Ch Clk Out 1)

This signal provides the clock signal for the pattern generator M8042A and AWG modules. Ch Clk Out 1 has to be connected to Ch Clk In 1 of the M8042A module.

Table 9. Channel clock output characteristics

Parameter	
Frequency range	4.0 to 60 GHz
Channels per module	1
Amplitude	Automatically adjusted for M8042A clock inputs
Frequency resolution	1 Hz
Frequency accuracy	±2 ppm typical (internal reference)
Data delay range	see M8042A
Intrinsic random jitter	10 mUI rms typical @ 58 GHz 6 mUI rms typical @ 32 GHz 8 mUI rms typical @ 16 GHz Refers to mUI of Ch Clk Out 1 frequency
Termination	50 Ω into GND. Do not operate into open. Unused outputs must be terminated
Coupling	AC
Connectors	1.85 mm, female

Channel clock output 2 (Ch Clk Out 2)

This output can be switched between two modes:

- Channel clock mode

This signal provides the clock signal for the second channel of the pattern generator M8042A. Ch Clk Out 2 has to be connected to Ch Clk In 2 of the M8042A module. Independent jitter profile for Ch Clk Out 2 compared to Ch Clk Out 1

- Forwarded clock mode

This signal is intended to be used to drive a DUT that requires a data rate divide by a second clock. It can contain identical jitter as the Ch Clk 1 Output 1. This clock signal is synchronous to the data pattern, phase relation will change when divider settings are modified.

Table 10. Channel Clock Output 2 characteristics in Channel Clock Mode

Parameter	Forwarded clock mode	PG module clock mode
Frequency range	2 to 32.4 GHz	4 to 32.4 GHz
Frequency divider factors	Symbol rate / clock divider n with n = 2, 4, 8, 16, 32	NA
Amplitude	0.5 to 1.2 Vpp typical, single ended	Automatically adjusted
Duty cycle	50%, accuracy ± 10% typical	50%, accuracy ± 10% typical
Intrinsic random jitter	10 mUI rms typical @ 16 and @ 32 GHz. Refers to mUI of Ch Clk Out 1 frequency	6 mUI rms typical @ 32 GHz 8 mUI rms typical @ 16 GHz Refers to mUI of Ch Clk Out 1 frequency
Data delay range	NA	see M8042A
Jitter delay range	±40 ns	±40 ns
Termination	50 Ω into GND. Do not operate into open.	50 Ω into GND. Do not operate into open.
Coupling	AC	AC
Connectors	1.85 mm, female	1.85 mm, female

Reference clock input (Ref Clk In)

This input allows locking the system clock to an external reference clock of 10 or 100 MHz instead of the internal oscillator.

Table 11. Reference clock input characteristics

Parameter	
Input amplitude	0.2 to 2.0 Vpp
Input frequency	
Reference mode	10 MHz or 100 MHz (±1%), sinewave or square wave
Direct mode	8 GHz – 16.2 GHz, sinewave or square wave, input amplitude is tbd
Clock multiplier mode	10 MHz to 16.2 GHz, sinewave or square wave
Termination	Single ended, 50 Ω, AC coupled
Connector	3.5 mm, female

Table 12. Reference clock multiplier characteristics. Requires M8009A-0G6

Ref clock input	Standard	Target symbol rate	Multiplier/divider	PLL loop bandwidth
100 MHz	PCIe	32 GBd PAM4	320	2 MHz
100 MHz	PCIe	16/ 32 Gb/s NRZ	160/ 320	2 MHz
100 MHz	PCIe	2.5/ 5.0/ 8.0 Gb/s NRZ	25/ 50/ 80	5 MHz
100 MHz	USB4 Gen 2 and 3	10/ 20 Gb/s NRZ	100/ 200	5 MHz
103.125 MHz	TBT3 Gen 2	10.3125 Gb/s NRZ	100	5 MHz
103.125 MHz	TBT3 Gen 3	20.625 Gb/s NRZ	200	5 MHz

Reference clock output (Ref Clk Out)

This signal provides a reference clock to lock with other instruments in the test setup.

Table 13. Reference clock output characteristics

Parameter	
CLK frequencies	10 MHz or 100 MHz (100 MHz is not available when using external 10 MHz Ref Clk In). Note: always derived from selected clock source, except in direct & clock multiplier mode. Then Ref Clk Out is derived from internal oscillator.
Amplitude	900 mVpp typical single ended into 50 Ω. square wave

Termination	50 Ω, nominal
Connector	3.5 mm, female

Reference clock output 16G (Ref Clk Out 16G)

This signal provides a clock between 8 and 16 GHz, relative to symbol rate.
It can be used as clock input or as trigger input for a precision time base of a DCA. Clean clock only.

Table 14. Reference clock output 16G characteristics

Parameter	
CLK frequency range	8 to 16.2 GHz
Amplitude	1100 mVpp sinusoidal nominal.
Intrinsic random jitter	150 fs rms typical
Termination	50 Ω, nominal
Termination voltage range	±500 mV typical
Connector	3.5 mm, female

Clock output 16G (Clk Out 16G)

This signal provides a reference clock for a DUT. It can be operated with jitter and without jitter. It provides a differential clock with adjustable amplitude, offset and termination. No phase alignment to data output.

Table 15. Clock output 16G characteristics

Parameter	
Frequency range	31.25 MHz to 8.1 GHz
Frequency divider factors	n * (1,2,3, to 256) n = 2, 4, 8
Amplitude	0.2 Vpp to 1 Vpp single ended into 50 Ω
Voltage window	-1.0 V to 3.7 V into 50 Ω
Duty cycle	50%, accuracy ±10% typical
Intrinsic random jitter	300 fs rms typical at 8.1 GHz clock divider = 1
Jitter injection	LF jitter • Can be set independently from Data Out • LF jitter parameters and range; same as for Data Out • Requires M8009A option -0G3 SSC • Same as Data Out

Termination	50 Ω into GND or external termination voltage. Do not operate into open.
Coupling	DC coupled, differential.
Connectors	3.5 mm, female

System trigger input A/B (Sys Trg In A, Sys Trg In B)

This signal is reserved for future use.

Table 16. System trigger input A/B characteristics

Parameter	
Input voltage	–1 V to +3 V
Termination voltage	–1 V to +3 V
Threshold voltage	–1 V to +3 V
Delay to data output	Tbd
Connector	3.5 mm, female

Synchronization input (Sync In)

This input is reserved for future use.

Table 17. Synchronization input characteristics

Parameter	
Cable required	M8199-61620. It is included in the M8042A-810 cable kit.
Connector	3.5 mm female

Synchronization output A/B/C (Sync Out A, Sync Out B, Sync Out C)

This output shall be only used with a M8042A module.

Table 18. Synchronization output A/B/C characteristics

Parameter	
Cable required	M8199-61620 (it is included in the M8042A-810 cable kit)
Amplitude	0.6 Vpp typical squarewave into 50 Ohm
Connector	3.5 mm female

Jitter Specifications

The M8009A has integrated and calibrated jitter sources. M8009A Option –0G3 is required.

Low-frequency jitter

Table 19. Specifications for low frequency periodic jitter (requires M8009A-0G3). Values shown are applicable at the data output of pattern generator remote heads M8058A and M8059A.

Parameter	Condition	Range
Amplitude range	For modulation frequencies of 100 Hz to 10 kHz:	0 to 8000 UI see table below.
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate < 3.95 GBd	0 to 20 MUI/s / Fmod
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate between 3.95 and 7.9 GBd	0 to 40 MUI/s / Fmod
	For modulation frequencies between 10 kHz and 40 MHz and symbol rate > 7.9 GBd	0 to 80 MUI/s / Fmod
Frequency range	100 Hz to 40 MHz, sinusoidal modulation	
Jitter amplitude accuracy	±2% ±1 ps typical	
Adjustable	For each data channel independently, same LFPJ for data and trigger. Clk Out 16G can be set independently.	

Table 20. Low frequency periodic jitter ranges.

Symbol rate	Max UI at modulation frequency 100 Hz to 10 kHz	Max UI at modulation frequency 10 MHz	Max UI at modulation frequency 40 MHz
2.0 to 3.95 GBd	2000 UI	2.0 UI	0.5 UI
3.95 to 7.9 GBd	4000 UI	4.0 UI	1 UI
7.9 to 120.00 GBd	8000 UI	8.0 UI	2.0 UI

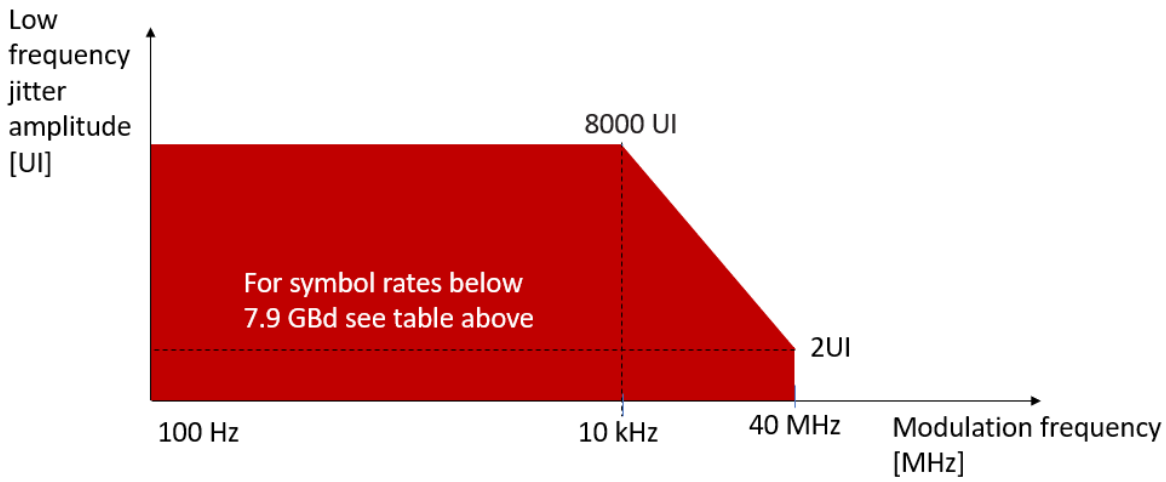

Figure 10. The multi-UI low frequency jitter range depends on selected baud rate and jitter modulation frequency. The graph shows the available range for symbol rates above 7.9 GBd when SSC is disabled.

High-frequency jitter

Table 21. High frequency jitter range (requires M8009A-0G3). This is the maximum sum of RJ, sRJ, HFPJ1, HFPJ2, and BUJ

For symbol rates	Applicable for	Range (minimum of)
≥ 7.9 GBd	sRJ/ RJ/ BUJ/ HF-PJ1/ HF-PJ2	1 UI. For 99 to 105 GBd : 0.3 UI [1]
3.95 GBd to < 7.9 GBd	sRJ/ RJ/ BUJ/ HF-PJ1/ HF-PJ2	0.5 UI
< 3.95 GBd	sRJ/ RJ/ BUJ/ HF-PJ1/ HF-PJ2	0.25 UI

1. For ambient temperatures <28 °C.

Table 22. Specifications for high frequency periodic jitter, random jitter, bounded uncorrelated jitter (requires M8009A-0G3).

Parameter		
High frequency periodic jitter (HF PJ1, HF PJ2)	Range	See HF jitter above [1]
	Frequency	1 kHz to 500 MHz. Two tone possible
	Jitter amplitude accuracy	±3 ps ±10% typical for symbol rates ≥ 32.5 GBd ±3 ps ±25% typical for symbol rates < 32.5 GBd
	Adjustable	For each channel independently
Random jitter (RJ)	Range	0 to 72 mUI rms max (1 UI p-p max) [1] See HF jitter above
	Jitter amplitude accuracy	±300 fs rms ±10% typical for symbol rates ≥ 32.5 GBd ±300 fs rms ±20% typical for symbol rates < 32.5 GBd
	Filters	High-pass: 10 MHz and "off", Low-pass: 100 MHz, 250 MHz, 500 MHz, 1 GHz
	Adjustable	For each channel independently
	Crest factor	14 (peak-peak to rms ratio)
Spectrally distributed RJ according to PCIe 2 (sRJ)	Range	0 to 72 mUI rms max (1 UI p-p max) [1]
	Frequency	LF: 0.01 to 1.5 MHz, HF: 1.5 to 100 MHz
	Jitter amplitude accuracy	±300 fs rms ±10% typical for symbol rates ≥ 32.5 GBd ±300 fs rms ±20% typical for symbol rates < 32.5 GBd
	Adjustable	For each channel independently
Bounded uncorrelated jitter (BUJ)	Range	See HF jitter above [1]
	PRBS polynomials	2^n–1, n = 7, 8, 9, 10, 11, 15, 23, 31
	Filters	50/ 100/ 200 MHz low pass 3rd order 150/ 300 MHz low pass first order (20 dB/ decade)
	Jitter amplitude accuracy	±5 ps ±10% typical for symbol rates ≥ 32.5 GBd ±5 ps ±20% typical for symbol rates < 32.5 GBd for settings shown in table below
	Rate for PRBS generator	625 Mb/s, 1.25 Gb/s, and 2.5 Gb/s
	Adjustable	For each channel independently
Clock/2 jitter	See M8042A data output	

1. Range of HF jitter applies to sum of RJ, HF-PJ1 and HF-PJ2, and BUJ. sRJ is mutually exclusive with RJ and BUJ. Valid if sRJ low pass filter is "on".

Table 23. BUJ accuracy applies for these conditions (requires M8009A-0G3).

Parameter [1]	Rate for PRBS generator	PRBS polynomial	Low pass filter
CEI 6G	1.25 Gb/s	PRBS 2^9–1	100 MHz
CEI 11G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
Gaussian	2.5 Gb/s	PRBS 2^{31}–1	100 MHz
CEI 25G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
CEI 56G	2.5 Gb/s	PRBS 2^{11}–1	200 MHz
IEEE 802.3 ck	2.5 Gb/s	PRBS 2^7–1 PRBS 2^9–1	150 MHz
IEEE 802.3ck	2.5 Gb/s	PRBS 2^7–1 PRBS 2^9–1	300 MHz

1. Other settings are not calibrated and do not necessarily generate the desired jitter histograms for all data rates of the PRBS generator.

Table 24. Specifications for spread spectrum clocking (SSC). SSC and segmented SSC are mutually exclusive. Requires M8009A-0G3 jitter modulation option.

Parameter		
SSC (spread spectrum clocking)	Symbol rate range for SSC	2 to 120.0 GBd
	Range [1] for center spread SSC	0 to 1% for symbol rates from 2 to 50.0 GBd For symbol rates from 50 to 120 GBd: max range is 50 GBd/ symbol rate * 1%. Example for 64 Gbd: max SSC deviation is 50/64 *1% = 0.78%
	Range [1] for asymmetric, downspread, upspread SSC: Upper deviation range Lower deviation range	0 to ± 1% for symbol rates up to 25 GBd For symbol rates from 25 GBd to 120 GBd: 25 GBd/ symbol rate * 1%. Example for 64 GBd: max SSC deviation = 25/64 *1% =0.39%
	Frequency	100 Hz to 200 kHz
	Modulation	Triangular and arbitrary modulation
	SSC amplitude accuracy	± 0.025% typical
	Outputs	Can be turned on/ off together for M8042A Data Out 1/2, Trg Out 1/2 and for M8009A Clk Out 16G and Channel Clk Out 1/2
Segmented SSC	Shape	Presets are available for: Universal Serial Bus (USB): USB4 10G, USB4 20G, USB4 40G, and

		DisplayPort (DP): DP RBR, DP HBR, DP HBR2, DP HBR3, DP UHBR10 User defined parameters: adjustable deviations from presets Custom: import of arbitrary waveforms for each segment
	Segments	Presets and user defined: 3 Custom: 1 to 4 Segment length: 32768 samples per segment
	SSC deviation range	See above range for asymmetric SSC
	SSC frequency	20 to 40 kHz
Residual SSC (rSSC)	Range	0 to 600 ps
	Modulation frequency	10 to 100 kHz
	Outputs	Can be turned on/off together for M8042A Data Out 1 and Trg Out 1 and for Data Out 2 and Trg Out2. Can be independently turned on/off for M8009A Clk Out 16G

1. Ranges are applicable when LF PJ and rSSC are turned off.

External Level Interference Sources

The Keysight M8054A interference source and M8194A, M8195A and M8196A AWG can be used as level interference source with sinusoidal and random modulation. The M8000 system software controls the interference parameters such as amplitude, bandwidth, crest factor. Keysight provides matched coupler pairs for injecting the RI or SI signal before and after the channel. See table below.

For more details, please refer to the datasheet for M8054A, M8195A, M8196A, M8194A.

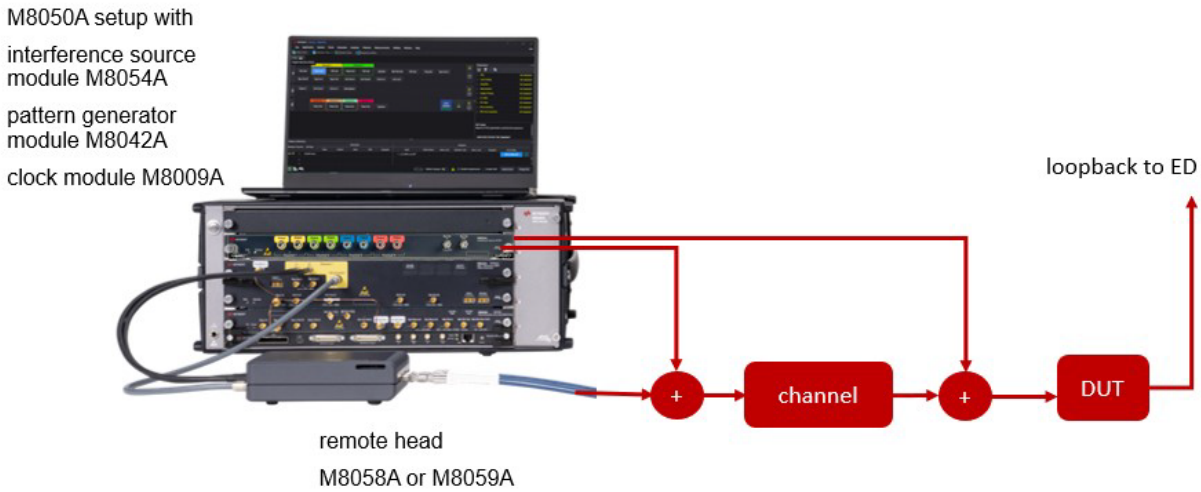

Figure 11. Keysight provides interference sources to be used in combination with M8050A to enable interference tolerance testing.

Table 25. Specifications for external level interference sources RI/SI with M8194A, M8195A, M8196A and M8054A.

Parameter	M8070B	M8194A	M8195A	M8196A/M8054A
Random Interference (RI)				
Random Interference (RI)		Yes	Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	0 mV to 800 mV, 1 mV resolution	0 mV to 1 V, 1 mV resolution	0 mV to 1 V, 1 mV resolution
	Lowest frequency range	230 kHz to 45 GHz	320 kHz -20 GHz (ch1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
	Highest frequency range	230 kHz to 45 GHz	320 kHz to 25 GHz	160 kHz to 32 GHz
	Crest factor (peak ratio)	> 5 [2]	> 5 [2]	> 5 [2]
Sinusoidal interference (SI)				
Sinusoidal interference (SI)		Yes	Yes	Yes
	Amplitude range (single ended, at DAC output of AWG)	0 mV to 800 mV, 1 mV resolution	0 mV to 1 V, 1 mV resolution	0 mV to 1 V, 1 mV resolution
	Frequency range	230 kHz to 45 GHz	320 kHz -25 GHz (channel 1 with deep memory: 100 Hz to 25 GHz)	160 kHz to 32 GHz
Common mode sinusoidal interference (CMSI)				
Common mode sinusoidal interference (CMSI)		Yes	Yes	Yes
	Amplitude	0 mV to 800 mV, 1 mV resolution	0 to 995 mV, 1 mV resolution	0 to 995 mV, 1 mV resolution
	Modulation frequency range	1 MHz to 12 GHz, one and two tone [1]	1 MHz to 12 GHz one and two tone [1]	1 MHz to 12 GHz, one and two tone [1]
	Phase range	-360 to 360 deg	-360 to 360 deg	-360 to 360 deg

Parameter	M8070B	M8194A	M8195A	M8196A/M8054A
Differential mode sinusoidal interference (DMSI)				
Differential mode sinusoidal interference (DMSI)		Yes	Yes	Yes
	Amplitude	mV to 800 mV, mV resolution	0 to 995 mV	0 to 995 mV
	Modulation frequency range	1 MHz to 12 GHz, one and two tone [1]	1 MHz to 12 GHz, one and two tone [1]	1 MHz to 12 GHz, one and two tone [1]
	Channel coupling	Yes, for channel 1 & 2, channel 3 & 4		
	Amplitude correction factor [3]	0 to 8.	0 to 10.	
	Phase range	-360 to 360 deg	-360 to 360 deg	-360 to 360 deg
Simultaneous injection of CMSI and DMSI	Simultaneous injection of CMSI and DMSI [1]	0 mV to 800 mV, 1 mV resolution	0 to 995 mV	0 to 995 mV
Accessories and software pre-requisites				
Recommended accessories	M8045A-802 Matched directional coupler pair, 1 to 50 GHz, 13 dB, 2.4 mm (recommended for RI and highest BW), M8045A-803 Matched coupler pair, DC to 40 GHz, 12 dB, 2.4 mm (recommended for PCIe5/6, CMSI, DMSI)			
Software pre-requisites	M8070B SW 7.0 or higher	M8194A FW 2.0.31.0 or later and M8070B SW 7.0 or later	M8195A firmware V3.2.0 or higher	M8196A firmware V2.1.0.0 or higher. For M8054A M8070B 6.5 or higher

1. Sum of amplitude in case of two-tone modulation must be within amplitude range
2. Requires M8070B software revision 7.2 or higher
3. Can be used to compensate for differences in channel losses in channel coupling mode

Emulation of ISI (Inter Symbol Interference)

Adjustable ISI (Intersymbol Interference) with M8070ISIB

The Adjustable ISI Software Package M8070ISIB simplifies receiver testing by offering the most flexible way for emulating channel loss for baud rates up to 120 Gbd. Up to a frequency range of symbol rate/ 2 a channel response can be emulated or de-embedded by the pattern generator by specifying a certain insertion loss at specific frequency points. This integrated channel emulation can be combined with actual physical ISI trace boards to result in a target test channel.

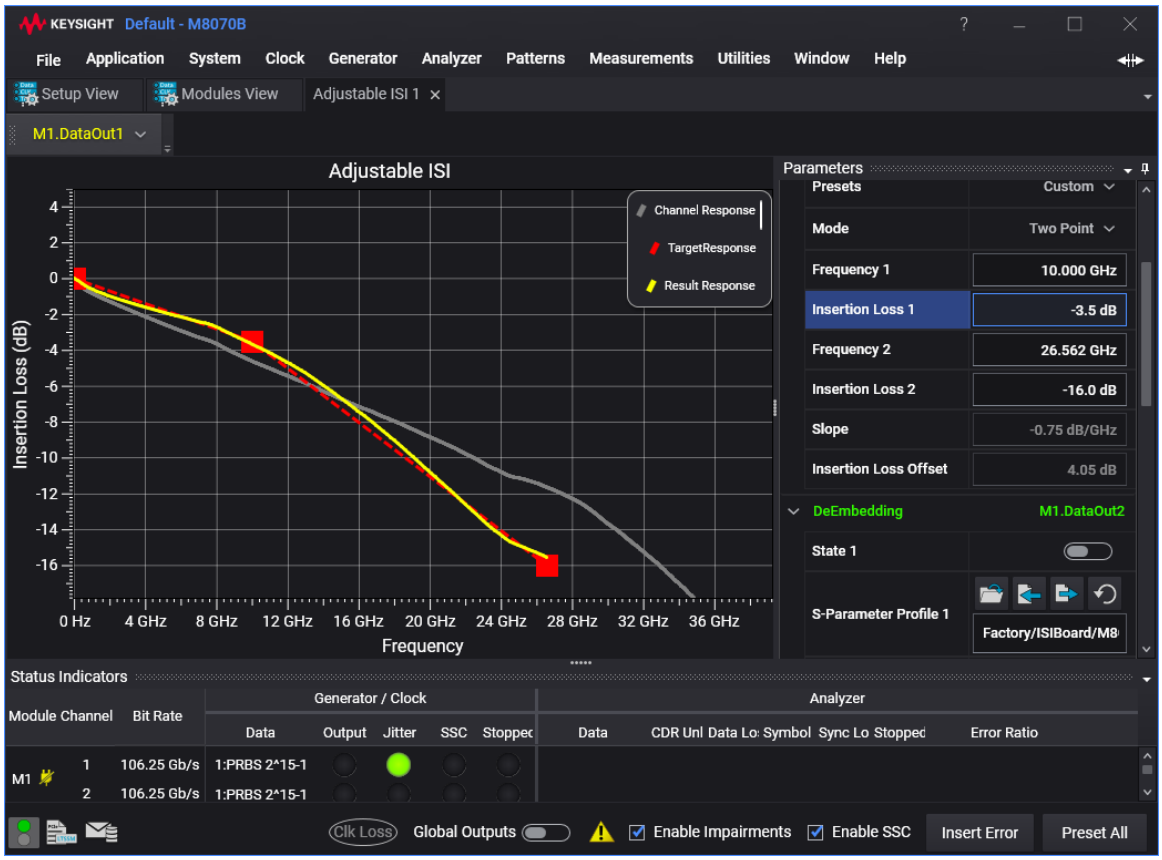

Figure 12: The adjustable ISI software package M8070ISI allows to emulate ISI internally with the M8042A pattern generator module. The example shows as channel response (gray) the insertion loss of an external ISI channel. You can add or remove insertion loss (red for target response) at 2 frequency points.

Table 26. Specifications for Adjustable ISI M8070ISIB when used with M8042A

Parameters	M8070ISIB	
Supported symbol rates	2.000 to 120.0 GBd for M8042A-G12 2.000 to 64.8 GBd for M8042A-G64 2.000 to 32.4 GBd for M8042-G32 A channel response can be emulated or de-embedded up to a maximum frequency range of symbol rate / 2.	

ISI modes	One Point Two Point S-Parameter from s2p or s4p file with adjustable weight	
ISI insertion loss	Range[1] at symbol rate / 2 Resolution Accuracy	-20 dB to +10 dB 0.1 dB 0.1 dB typical
De-embedding	Up to two s2p or s4p files with adjustable weight	
Software download	For latest version see: https://www.keysight.com/us/en/support/M8070ISIB/adjustable-isi-channel-emulation-package-m8000-series-ber-test-solutions.html#drivers	
License types	Choose between node-locked, transportable, network, USB-dongle license types either perpetual or with limited duration. The network license is only recommended when using multiple M8050A setups within one company	
Pre-requisites	Requires M8042A pattern generator module with de-emphasis option (M8042A-0G4) M8070B software revision 9.5.350.6 or higher M8070ISIB software revision 1.0.100.6 or higher M8042A module driver 2.5.50.0 or higher	

1. The available loss range is referenced to the defined external ISI board or 0 dB if the external ISI board is set to NONE. It scales linearly from 0 Hz to symbol rate/ 2.

ISI Channel Boards

Figure 13. Keysight offers ISI channel boards M8049A-001, -002, and -003 that allow emulating a wide range of channel losses.

Please refer to the M8049A data sheet for more details.

Error Analysis

The M8046A error analysis module can be used in combination with the M8042A pattern generator.

Please see the M8040A datasheet for M8046A specifications.

Measurements

Table 27. Measurement capabilities for M8050A when using M8042A with M8046A. (For measurements with UXR see table below)

Measurement		M8070B	M8070ADVB with M8046A	M8070EDAB with M8046A
BER, SER	Accumulation and instantaneous	Yes		
Counters	Compared bits, errored bits Compared 0 bits, errored 0 bits Compared 1 bits, errored 1 bits Compared symbols, errored symbols Compared symbols 0, 1, 2, 3 Errored symbols 0, 1, 2, 3	Yes		
Jitter tolerance		No	Yes	
BER scan with RJ, DJ separation		No	Yes [1]	
Output level and Q-factor		No	No	
Sampling point view		Yes		
BER versus parameter automated sweep		No	Yes	
Error distribution analysis	See M8070EDAB details below.	No	No	Yes
Pattern capture		Yes		
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.	Yes		
Eye diagram		No	No	No

1. The measurement is available in the user interface, but just for debugging/troubleshooting purposes. The accuracy of jitter separation results is unspecified in case of NRZ and invalid in case of PAM4 signals.

Specifications for Error Analysis of Signals above 58 GBd based on Infiniium UXR Series Oscilloscopes

For analyzing errors of PAM4 up to 58 GBd, the M8046A error analyzer module can be used. Please see the M8040A datasheet for details. For symbol rates above 58 GBd, the Keysight M8000 system software supports the use of Keysight real-time oscilloscopes for capturing the signal and decoding it into a pattern stream. The M8000 system software uploads the acquired pattern and handles the synchronization and comparison with the expected pattern, even for long PRBS polynomials such as PRBS31Q. This method allows measuring target BERs of up to of 10^{-6} for symbol rates up to 120 GBd within measurement times of about 1 minute. The real-time oscilloscope provides uniquely adjustable equalization and an integrated clock recovery supporting symbol rates up to 120 GBd.

See table below for more details.

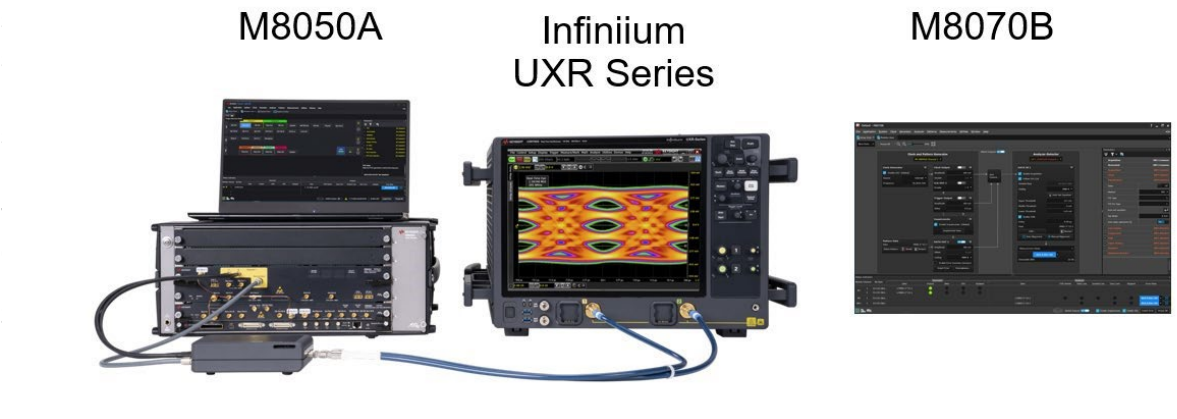

Figure 14. The M8070ADVB controls the UXR and uploads the decoded pattern streams for synchronization and comparison with expected patterns.

Table 28. Conditions for error analysis with M8070ADVB using a real-time oscilloscope for symbol acquisition

Parameter	Description
Supported real-time oscilloscope models	Keysight UXR series, all models from 59 to 110 GHz (2 or 4 channels)
Symbol rates	Maximum symbol rate is limited by UXR model: 14 GBd to 60 GBd for UXR0402/4A 14 GBd to 75 GBd for UXR0502/4A 14 GBd to 96 GBd for UXR0592/4A, UXR0592/4AP 14 GBd to 105 GBd for UXR0702/4A, UXR0702/4AP 14 GBd to 120 GBd for UXR0802/4A 14 GBd to 120 GBd for UXR1002/4A 14 GBd to 120 GBd for UXR1102/4A
Hardware acceleration	Hardware acceleration is active for 256 GSa/s UXR models when parameters are set in M8070ADVB to meet all of the following conditions: - Symbol rate: 51.2 GBd to 120 GBd - CDR type: 2nd order PLL - CDR loop bandwidth: Symbol rate / 2655 to Symbol rate/ 1000 Measurements are - 1.8 times faster (meas.) for JTOL measurements - 2.5 to 3.5 times faster (meas.) for BER measurements when hardware acceleration is active. Display shall be turned OFF to achieve fastest measurement times. Factor of acceleration depends on parameter settings of the UXR such as e.g., line coding, baud rate, bits per acquisition and is provided as an estimation.
Target BER	Hardware acceleration active: -10^{-7} Hardware acceleration inactive: -10^{-6}
Coding	NRZ, PAM4, PAM6, PAM8
Pattern capture	Yes
Masking	Expected bits can be masked (ignored) during error counting. Bitwise and block-wise masking is possible.
Expected patterns	User definable: PRBS 2^n-1 with n = 7, 9, 10, 11, 13, 15, 23, 31, 33, 35, 39, 41, 45, 47, 49, 51 Memory patterns with max. pattern length of 256 kbit
Measurements	• Jitter tolerance, BER and SER

Parameter	Description
	• Error distribution analysis (restrictions with respect to memory depth of UXR to be able to capture maximum frame length may apply) • Automated parameter sweep versus BER
Measurement time	Depends on: • Expected pattern type • Expected pattern length (in case of memory patterns) • Symbol rate • Equalizer usage and parameters • Acquisition depth in UI • Target BER and confidence level
BER and symbol counters	BER counters: • Compared bits • Errored bits • Compared 0 bits, compared 1 bits • Errored 0 bits, errored 1 bits Symbol counters: • Compared symbols • Errored symbols For each symbol level: • Compared symbols • Errored symbols

Parameter	Description
Parameters	Acquisition Number of bits per acquisition. (Note: The maximum number of bits per acquisition is limited by the oscilloscope's acquisition memory depth, symbol rate and clock recovery setting.) • Global acquisition bandwidth limit • Channel bandwidth limit and filter type • Pattern capture up to 100 Mbit Horizontal reference clock: internal, external 10 MHz and 100 MHz Clock: Follow Sys Clock, symbol rate Line Coding: • Coding (NRZ, PAM4, PAM6, PAM8) • Symbol mapping (uncoded, Gray, custom) • Custom symbol mapping Comparator: • Compare mode (single ended / differential) • Polarity (non-inverted / inverted) • Auto-set thresholds • User-defined thresholds Equalizer FFE- Number of taps • FFE- Number of pre-taps • FFE - Auto-set coefficients • CTLE - DC gain • CTLE - Frequency pole #1, Frequency pole #2, • CTLE - Frequency zero #1 • DFE- Taps • DFE-Auto-set coefficients Clock Recovery (2nd Order CR) • Loop bandwidth • Symbol rate divider • Damping factor Sample delay (PAM4 only) Auto alignment • Covers thresholds, sample delay and equalizer coefficients Automatically set scope parameters: • Thresholds • FFE coefficients (cannot be changed by user) • Sample delay position (in case of NRZ)
Software pre-requisites	UXR: Infiniium version 11.40.00202 or higher and M8070B: M8000 system software revision 9.5.350.6 or higher

Parameter	Description
	M8070ADVB advanced measurement package software revision 1.9.150.4 or higher
Measurement packages	Following licenses are required on the oscilloscope in addition: • D9010PAMA Pulse Amplitude Modulation PAM-N analysis software • D9020ASIA Advanced signal integrity software (EQ, InfiniSim, Advanced crosstalk)
Connection to UXR	LAN recommended

User interface and remote control

The M8070B system software for M8000 series of BER measurement solutions is required to control the M8050A BERT. The user interface supports controlling combinations of M8050A and with other hardware of the M8000 Series.

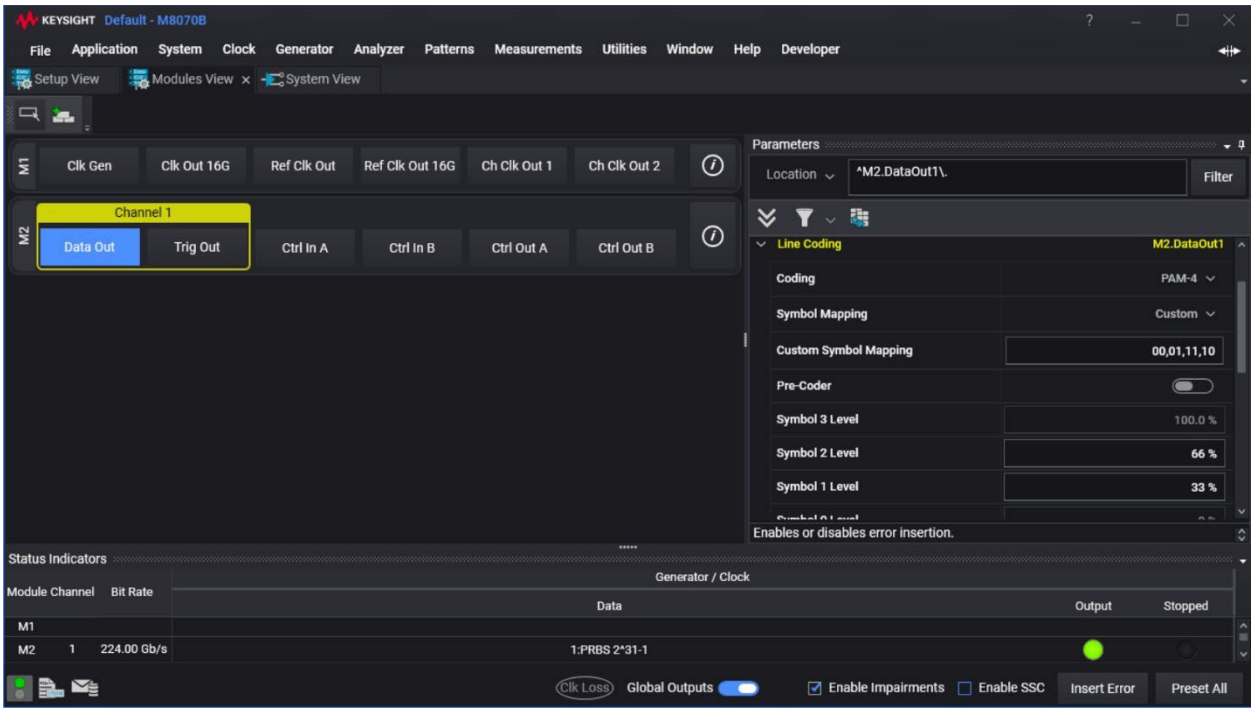

Figure 15. The M8070B system software is required to control the M8050A high-performance BERT. The user interface provides control of all parameters. It provides a graphical user interface and remote control via SCPI. Shown is a preliminary version of the module view with M8009A clock module (M1) and M8042A pattern generator module (M2).

M8070B system software for the M8000 Series of BER measurement solutions

Table 29. User interface and remote-control interface M8070B

Parameter	
Programming language	SCPI
Remote control interface	LAN
Save/Recall	Yes
Software update	Under the help menu the M8070B can show if there are newer SW revisions of M8070B, M8070ADVB, M8070EDAB, M8070ISIB, and M8042A, M8009A module driver packages available for download from K.com.
SCPI recorder	Allows recording of the SCPI commands that correspond to the interactive control in the GUI. This includes: • Parameter changes • Sequence and pattern configuration • Measurement creation, configuration and execution • Group configuration • Save and recall of settings The recorded SCPI commands can be copied to the clipboard or saved to a file for later playback.
Software download	For latest version of M8050A module drivers see: https://www.keysight.com/us/en/support/M8050A/120-gbd-high-performance-bert.html#drivers For latest version of M8070B system software see: https://www.keysight.com/us/en/lib/software-detail/computer-software/m8070b-system-software-3021035.html
Offline version	Yes. Can be used without M8000 hardware connected.
License types	Not licensed. Free baseline software

M8070ADVB advanced measurement package

Table 30. Features of the advanced measurement software package M8070ADVB

Advanced measurements	M8070ADVB
Measurements	See table measurements
Export of measurement results	Jitter tolerance results as *.csv file
Controlling other instruments via M8070B	Real-time oscilloscopes, e.g. DASZ634A, UXR0804A DCA oscilloscopes, e.g. N1046A, N1060A
Scripting interface	The built-in scripting engine is based on IronPython. It enables the control of the device under test as well as another test equipment. Function hooks are available to tailor your measurements, such as read-out of built-in error counters or initializing the device
DUT control interface	Enables access to built-in error counters and status registers of a device under test (BIST) for use with automated measurements like accumulated BER and jitter tolerance. Can also be used to customize the measurements to DUT specific needs. IronPython scripting and .net libraries are supported to interface with the DUT
Auto-optimizing de-emphasis taps	DE taps are calculated for best eye height. Can be combined with embedding/de-embedding of s-parameter files. Supported DCA models: N1060A, N1094A/B, 86108B, N1046A.
Software download	For latest version see: https://www.keysight.com/us/en/support/M8070ADVB/advanced-measurement-package-m8000-series-bert-test-solutions.html#drivers
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with 6/12/24 month duration. The network license is only recommended when using multiple M8050A setups within one company

M8070EDAB error distribution analysis package

Table 31. Features of the error distribution analysis package M8070EDAB

Error distribution analysis	M8070EDAB
Measurements	• Frame loss ratio estimation • Error map • Symbol-errors per frame distribution • Consecutive error distance distribution

Software download	For latest version see: https://www.keysight.com/us/en/support/M8070EDAB/error-distribution-analysis-m8000-series-bert-test-solutions.html#drivers
License types	You can choose between node-locked, transportable, perpetual license, network, USB-dongle license types with 6/12/24 month duration. The network license is only recommended when using multiple M8050A setups within one company

Table 32. System requirements for M8050A and M8070B System Software

Parameter	
M9537A 1-slot AXIe embedded controller requirements	Choose M8050A-BU3 or -BU5 for a pre-installed embedded controller M9537A including pre-installation of M8070B software and module licenses. M8050A-BU3 and -BU5 are pre-configured with Windows 10. Otherwise: M9537A 1-slot AXIe embedded controller, choose options for Windows 10, 8 or 16 GB RAM, SSD.
External PC	Connection to AXIe chassis: • USB 2.0 (Mini-B) recommended or • PCIe 2.0/8x (only for highest data throughput and desktop PC) or • Thunderbolt (only for M9506A) Memory: Minimum of 8 GB RAM recommended
Operating system	Windows 10, 64-bit, Version 1607 (Anniversary Update) or newer
Display resolution	Minimum requirement 1024 x 768
Software pre-requisites	Keysight IO Libraries Suite 2022 (build 18.2.27313.1) or above M9505A AXIe 5-slot chassis firmware: Version 2.1.5 or above M9502A AXIe 5-slot chassis firmware: Version 2.1.5 or above M9506A AXIe 5-slot chassis firmware: Version 1.0.473.1 or above M8070B, M8070ADVB, M8070EDAB: Version 9.5 or above M8009A and M8042A module drivers: Version 2.0 or above

General Characteristics and Physical Dimensions

General characteristics for M8050A

Table 33. General characteristics for M8042A, M8009A modules and M8058A, M8059A remote heads.

Parameter	
Operating temperature	5 °C to 35 °C
Storage temperature	–40 to +70 °C
Operating humidity	15 to 95% relative humidity at 40 °C (non-condensing)
Storage humidity	24 to 90% relative humidity at 65 °C (non-condensing)
Operating altitude	Up to 3000 m
Physical dimensions	See tables below
Weight net	See tables below
Weight shipping	See tables below
Power consumption	See tables below
Interface to controlling PC	PCIe or USB or Thunderbolt
Recommended recalibration period	2 years
Warm-up time	30 minutes
Cooling requirements	Slot air flow direction is from right to left. When operating the M8050A choose a location that provides at least 80 mm of clearance at each side. See also start-up guide for M9505A chassis.
EMC tested acc. to	IEC 61326-1
Safety tested acc. to	IEC61010-1, ANSI/UL61010, CSA22.2 No. 61010-1
Quality management	ISO 9001, 14001

Physical dimensions and power for M8042A

Table 34. Physical dimensions and power requirements of the M8042A pattern generator module

	M8042A-0G1 (1 channel version)	M8042A-0G2 (2 channel version)
Form factor	2-slot AXIe module	3-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 61 mm x 315 mm	351 mm x 92 mm x 315 mm
Power requirements	300 W (nom.)	600 W (nom.)
Weight net	6.1 kg	8.5 kg
Weight shipping	9.6 kg	12.0 kg

Physical dimensions for M8058A and M8059A

Table 35. Physical dimensions and power requirements of the M8058A and M8059A generator remote heads

Parameter	
Physical dimensions (W x H x D)	150 mm x 90 mm x 44 mm (remote head without cables)
Physical dimensions for remote head with cable	Length of cable connection between M8058A/M8059A and M8042A module: 60 cm
Weight net	1.0 kg
Weight shipping	Shipment of one Remote Head 3.7 kg Shipment of two Remote Heads 4.7 kg

M8042A 600 mm M8058A 150 mm, 1.85mm cable

M8042A 600 mm M8059A 150 mm, 1.0 mm cable

Physical dimensions and power requirements for M8009A

Table 36. Physical dimensions and power requirements of the M8009A clock module

Form factor	1-slot AXIe module
Physical dimensions (W x H x D)	351 mm x 30 mm x 315 mm
Power requirements	200 W (nom.)
Weight net	2.7 kg
Weight shipping	6.5 kg

Physical dimensions for M8050A-BU2, -BU3, -BU4, and -BU5 bundles with AXIe chassis

Table 37. Physical dimensions and power for M8050A bundles with AXIe chassis

Parameter	
Form factor	Modules are pre-installed in M9505A 5-slot AXIe chassis
Physical dimensions (W x H x D)	Depth including semi-rigid cables without remote heads: M8050A-BU2 / -BU3: 462 mm x 193 mm x 485 mm M8050A-BU4 / -BU5: 462 mm x 384 mm x 485 mm
Weight net	Without modules, without packaging material, without filler panels: M8050A-BU2: 13.3 kg (M9505A) M8050A-BU3: 2.9 kg (M9537A) +13.3 kg (M9505A) M8050A-BU4: 26.6 kg (2 x M9505A) M8050A-BU5: 2.9 kg (M9537A) + 26.6 kg (2 x M8050A-BU3)
Weight shipping	Weight per system package only (wo chassis, wo modules) M8050A-BU2 / -BU3: 12.3 kg M8050A-BU4 / -BU5: 24.6 kg (2 x M8050A-BU2)

Specification Definitions

All specifications in this revision of the data sheet are preliminary.

If not otherwise stated all outputs need to be terminated with 50 Ω to GND.

All M8042A specifications if not otherwise stated are valid after the remote heads and at the end of the matched reference cable pair. The reference cable is M8058A-801 when used with M8058A remote head and cable M8059A-801 when used with the M8059A remote head.

Specification (spec.)

The warranted performance of a calibrated instrument that has been stored for a minimum of 2 hours within the operating temperature range of 0 °C to 40 °C and a 15-minute warm up period. Within ±10 °C after auto calibration. All specifications include measurement uncertainty and were created in compliance with ISO-17025 methods. Data published in this document are specifications (spec) only where specifically indicated.

Typical (typ.)

The characteristic performance, which 80% or more of manufactured instruments will meet. This data is not warranted, does not include measurement uncertainty, and is valid only at room temperature (approximately 23 °C).

Nominal (nom.)

The mean or average characteristic performance, or the value of an attribute that is determined by design such as a connector type, physical dimension, or operating speed. This data is not warranted and is measured at room temperature (approximately 23 °C).

Measured (meas.)

An attribute measured during development for purposes of communicating the expected performance.

This data is not warranted and is measured at room temperature (approximately 23 °C).

Accuracy

Represents the traceable accuracy of a specified parameter. Includes measurement error and time base error, and calibration source uncertainty.

Related Keysight Literature

Description	Pub number
M8050A high-performance BERT 120 GBd - configuration guide	3122-1285EN
M8040A high-performance BERT 64 GBd - data sheet	5992-1525EN
M8054A interference source - data sheet	5992-3917EN
M8049A ISI channel boards - data sheet	5992-3617EN
M9505A AXIe chassis 5-slot - data sheet	5990-6584EN
M8047A Redriver - data sheet	3120-1399EN
M8047B Redriver - data sheet	3122-1648EN
N5991 Receiver compliance test automation platform - data sheet	5992-4365EN
M8091CKCA Receiver test application for IEEE802.3ck - data sheet	3122-2122EN
BER measurements using a real-time oscilloscope controlled from M8070B system software – application note	5992-2676EN
Advanced modulation and coding challenges – white paper	5992-3021EN
Equalization: the correction and analysis of degraded signals – white paper	5989-3777EN
Error analysis of PAM4 signals – application note	5992-3268EN
Conformance testing of 800G Ethernet links for data center 100G/lane test solution – application note	3121-1220.EN

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