

# M5400PLSA

## Quantum Library Dynamic Pulse Generation

### Overview

The M5400PLSA allows quick and easy access to targeted quantum synthesizer and modulation FPGA IP blocks used within PathWave FPGA to create qubit pulses with minimal to no latency with real time-controlled waveform execution optimized to be used with the M3202A hardware platform.

### The M5400PLSA software package

This licensed software package for the quantum library includes a quantum M5400PLSA programming API that directly interacts the SD1 3.X driver communication, KS2201A PathWave Test Sync Executive and Quantum FPGA IP library for a user friendly programming environment that can quickly be used for superconducting qubit control and readout applications.

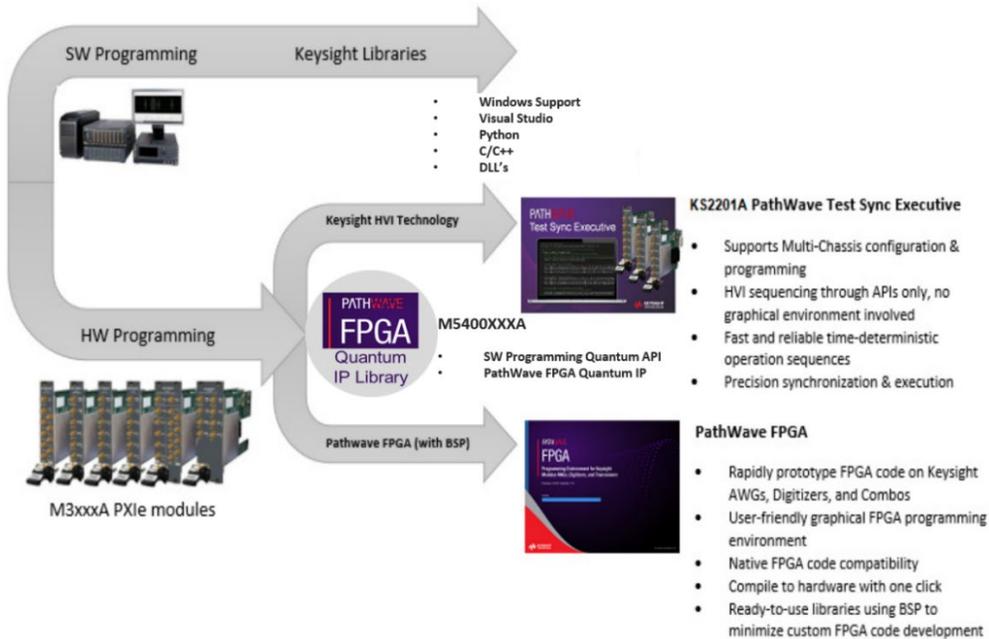


Figure 1. M5400PLSA operation flow

Using the fully integrated software and FPGA Gateway package allows for simplifying your configuration and provides massive savings of development time to integrate and expand to multi qubit systems including multi-chassis configurations for scaling system configurations.

## What is included?

Feature	Description	Includes	Licensing
M5400PLSA	Quantum Library Pulse Generation	Quantum Library API, PathWave FPGA Quantum IP Library	Run-time per PXIe Instrument Module

## Features

The quantum FPGA IP provides ultra-light weight and scalable components that have a small FPGA footprint that allows for 0ns latency pulse waveform execution and play using precise real-time control through PathWave Test Sync Executive technology known as HVI, hardware virtual instrument. The convenient quantum FPGA IP also provides the ability to phase lock to the M3102A Digitizer through HVI. Using precise real-time control allows for deterministic phase coherent simultaneous waveform selection and triggering of launching arbitrary pulse waveforms with no latency nor requires pre-determined order of waveform playing.

- GaplessAgileAWG - Dual Port Digital synthesizer with programmable memory length to accommodate custom configurations of waveform length for up to 64 waveforms with dynamic length allocation if not all 64 waveforms are defined. Convenient and flexible for qubit pulse generation for readout and control applications.
- DUC - Digital Up Converter for applying amplitude and phase modulation to the waveform synthesizer outputs with the convenience to create real time control of amplitude, phase, offset and frequency to modulated outputs for qubit readout and control applications.
- QuWaveControl used to provide easy control to launch waveforms independently or simultaneously across all channels controlled all through a HVI sequence, host software or PXI trigger hardware interface.

Table 1-1: Technical Performance Specifications (IP Components)

IP Component	Nominal Characteristics					
	Parameter	Min.	Typ.	Max.	Units	Comments
<b>GaplessAgileAWG</b>						
	Waveform Port A		160		bits	Data output width compatible with DUC awgAngle input. Normalized real phase, complex I quadrature, or complex polar phase
	Waveform Port B		80		bits	Data output width compatible with DUC awgAmplitude input. Normalized real amplitude, complex Q quadrature, or complex polar amplitude
	Waveforms	1		64	waveforms/port	6-bit decode waveform selection to scale up to 64 selectable waveforms
	Memory Address Size	11	14	16	bits	address width to specify memory size. Applied to both waveform ports settable in PathWave FPGA instantiation parameter
	Max Memory Samples	10,240	81,920	327,680	samples/port	per Memory Address. Size setting

IP Component	Nominal Characteristics					
	Max Waveform Samples	160	1,280	5,120	samples/max waveforms	per Memory Address. Size setting and all 64 waveforms specified
	Minimum Waveform Sample Size	10	10	10	Samples	10ns length. See Nominal Characteristics. Sampling Clock. (Comments in the section below.)
	Output Latency		0		ns	from waveform selection trigger event using QuWaveControl
	Buffered Early Waveform Selection / Trigger Event		1		trigger	allows for single buffered waveform selection trigger event. Executes 0ns after current waveform execution completes.
	Re-arm time		0		ns	allows for gapless waveform generation using HVI instruction. No real-time HVI phase, amplitude, frequency within seq.
<b>DUC</b>						
	Amplitude	-1.5		1.5	volts	amplitude of modulating signal. Control via Quantum Library API or HVI instructions.
	DC Offset	-1.5		1.5	volts	dc offset of modulating signal. Control via Quantum Library API or HVI instructions.

IP Component	Nominal Characteristics					
	Parameter	Min.	Typ.	Max.	Units	Comments
	Frequency	-400		400	MHz	frequency of modulating signal. Control via Quantum Library API or HVI instructions
	Phase	-180		180	degrees	phase of modulating signal. Control via Quantum Library API or HVI instructions
<b>QuWaveControl</b>						
	Number of Waveform Control Ports		4		waveform selection and auto trigger	Individually programmable to control independently or simultaneously for waveform generation across channels
	Waveform Selection		6		bits	6-bit decode for 64 waveforms
	Auto Trigger		1		bit / waveform selection	1-bit auto trigger generated upon executing waveform selection command either HVI or SW host
	PXI Trigger		1		bit / waveform selection	1-bit auto trigger event from PXI Trigger rising edge event
	Waveform Selection Options		3		interfaces	HVI, SW Host or PXI Triggers for waveform selection interfaces supported

**Table 1-2: Technical Performance Specifications (SD1 3.X Programming)**

Component IP Interfaces	Modulation Support			Comments
	AM	PM/FM	IQ	
				Documentation reference: <a href="#">M320XA / M330XA AWG User Guide</a>
FuncGen_Control		✓	✓	enable phase, quadrature IQ modulation via SD1 3.X programming interface
ModGain_Control	✓		✓	enable amplitude, quadrature IQ modulation via SD1 3.X programming interface

**Table 1-3: Technical Performance Specifications (Sandbox Interfaces)**

Sandbox Interfaces	Nominal Characteristics					
	Parameter	Min.	Typ.	Max.	Units	Comments
Sampling Clock	Clock		200		MHz	5 samples/clock (5 ns)
System Reset	nRst		5		ns	active low sandbox system reset

**Only key parameters listed in the Tables; not all inclusive:** Only key quantum IP components have been listed in the Tables above. Many other complementing IP components are included in the quantum IP library. Many sandbox interfaces and off-the-shelf IP components included with PathWave FPGA are not listed here.

**Table 2: Utilization Data**

Limiting Factors	Utilization			
	Pulse Generation Resource Considerations -k41 target 4 Channel M3202A			
Component	BRAM	DSP	LUT	Notes
DUC	2.5	42	1508	Enables Modulation and other key parametric attributes
GaplessAgileAWG	80	0	3195	Pulse Generation up to 64 waveforms; Memory Address size set to 14 (default)
	10	0	3121	Pulse Generation up to 64 waveforms; Memory Address size set to 11 (min)
1 channel IF qubit pulse generation	82.5	42	4703	x1 DUC x1 GaplessAgileAWG. Memory Address size set to 14 (default)

Limiting Factors	Utilization			
2 channel IQ qubit pulse generation	85	84	6211	X2 DUC x1 GaplessAgileAWG. Memory Address size set to 14 (default)
<b>Channel Configurations (330 BRAM max, 660 DSP max per -k41 playground)</b>				
Memory Address Size				
4 Qubit IF (4 channels)	330	168	18,812	Single GaplessAgileAWG per channel. Memory Address size set to 14 (default), 4 DUC's
2 Qubit IQ (4 channels)	170	168	12,422	Single GaplessAgileAWG shared between two channels for IQ. Memory Address size set to 14 (default), 4 DUC's
12 Qubit IF (4 channels)*	150	504	55,548	GaplessAgileAWG. Memory Address size set to 11 (min). 12 DUC's 3 Qubits per channel
6 Qubit IQ (4 channels)*	90	504	36,822	Assumes one shared GaplessAgileAWG per channel pair per qubit. Memory Address size set to 11 (min). 2 DUC's per channel pair per qubit. 3 qubits per paired channels

\* Frequency Division Multiplexed models (12 qubit, 6 qubit configurations) do not include adder stage to output in utilization calculation.

## PathWave FPGA Use Model

Create custom FPGA designs within your own partitioned FPGA space known as a "sandbox" within a supported PathWave FPGA enabled PXIe instrument.

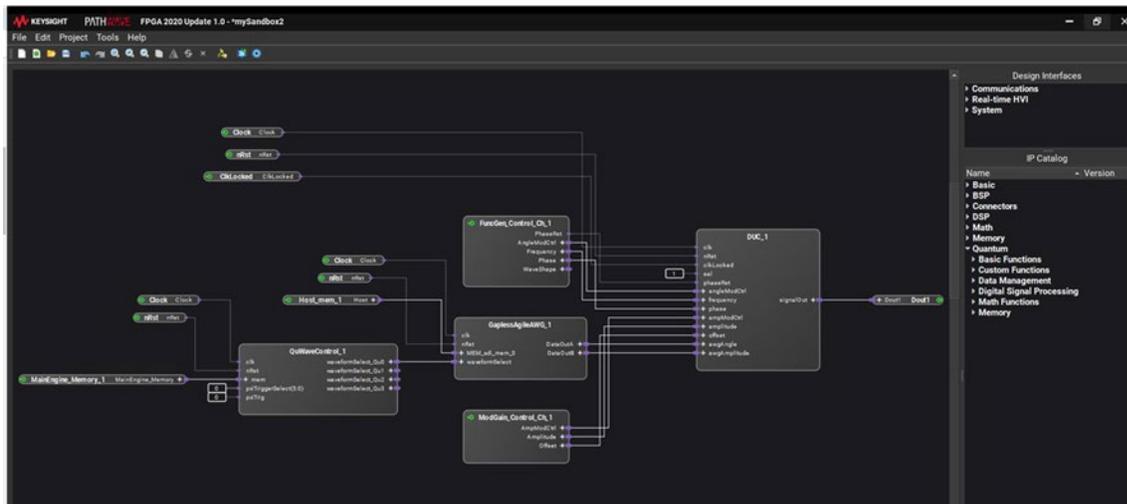


Figure 2. PathWave FPGA use model

You can easily integrate ready-to-use off-the-shelf custom quantum FPGA IP blocks to create control and readout pulses for many qubits in a single schematic with no Gateway HDL programming knowledge required.

## Procurement information

Products	Model Number
M5400PLSA Pulse Generation	M5400PLSA
Dependencies	
KS2201A PathWave Test Sync Executive	KS2201A
KF9000A PathWave FPGA Programming Environment	KF9000A
M3202A PXIe Arbitrary Waveform Generator, 1 GSa/s, 14 bit, 400 MHz -K41 -HV1 CLF (SD1 3.X driver)	M3202A

## Licensing terminologies

Terminology name	Description
Subscription	Subscription licenses can be used through the term of the license only (6, 12, 24, or 36 months).

## Licensing types

License type	Description
Node-locked	License can be used on one specified instrument/computer.
Transportable	License can be used on one instrument/computer at a time but may be transferred to another using Keysight Software Manager (internet connection required).
USB Portable	License can be used on one instrument/computer at a time but may be transferred to another using a certified USB dongle (available for additional purchase with Keysight part number E8900-D10).
Floating (single site, regional, or worldwide)	Networked instruments/computers can access a license from a server one at a time. Multiple licenses can be purchased for concurrent usage.

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## Ordering Information and Related Literature

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