#### DATA SHEET

# D9040EDPV Embedded DisplayPort Electrical Performance Validation Software

The Keysight Technologies, Inc. eDP electrical performance and Validation (EPV) software for Infiniium Series oscilloscopes (see Ordering Information table below) provides you with a fast and easy way



to verify and debug your eDP interface designs for embedded systems. The eDP Electrical Performance Validation software is designed to be uniquely flexible to handle the wide variety of configurations that are possible in embedded systems and pose characterization challenges. It offers the standard tests that are recommended as well as other informative tests, so it functions equally well as a validation tool. It displays the measurement data results in a flexible report format, and the report also provides a margin analysis that shows how closely your device passed or failed each test.

To make measurements with the eDP EPV software, you will also need an eDP TPA fixture for highspeed signal access as well as for AUX channel and other lines of the interface. Available fixtures are identified in the Test Accessories table below.

The eDP EPV software is based broadly on the widely-industry-accepted Keysight DisplayPort D9040DPPC compliance application, which extends utility to include a wizard graphic user interface that enables test selection, parameter election, test specification entry, and test template sharing. These features are unique in the industry and are supported to enable ecosystem sharing of test process specifics for highly variant embedded designs.

There is no official interoperability program for eDP, though this software goes a long way to create a defacto program – if only for a specific product or family of products. The default specifications are those found in the VESA<sup>1</sup> test guideline eDP PHY CTG v1.0. The tests available in the eDP EPV software package are identified in Table 1. However, there is no limit to what tests you can have available with the Infiniium framework add-in feature, with which you can add your own tests or tests from colleagues to the test suite offered. Details of the add-in capability are covered in the Extensibility section below.



<sup>1</sup> Video Electronics Standards Association (www.vesa.org)

## Features

The eDP Electrical Performance Validation software offers new and unique capabilities as well as the standard features available with all Keysight Infiniium framework applications:

- Full physical layer testing of high-speed lanes
- Verification of link layer physical layer control
- Test status tracking
- Measurement process configurability
- Automated scope measurement setup
- Bit rate parameters: Nominal value of bit rate, number of bit rates and test line limit for frequency accuracy
- Level parameters: Nominal value of level, number of levels and test line limits for level accuracy or value of relative change between level settings
- Pre emphasis parameters: Nominal value of pre-emphasis, number of preemphasis settings and test line limits for pre-emphasis accuracy or value of relative change between pre-emphasis settings
- Eye diagram mask testing: Entry of arbitrary mask through mask files vs. bit rate
- Jitter testing: entry of arbitrary RJ, DJ, TJ values vs. bit rate
- Test plan creation: Selection of device conditions to test
- Test template: Create default templates for device types avoiding re-entry and share complete test process setup with others for consistent settings for same process requirements in different locations
- Test results reports with pass/fail margin analysis

With the eDP EPV test software, you can finally solve the myriad of test issues that embedded test systems present with one application.

## Easy test process definition

The eDP Electrical Performance Validation software extends the ease-of-use advantages of Keysight's Infinitium Series oscilloscopes and previous DisplayPort standard test software to testing eDP designs.

The application will guide you through device setup and test connection with setup wizards to capture all the test process details. In doing so, you will create a tailored process to validate or characterize your device and get exactly what you need.

## Using the eDP Electrical Performance Validation Software

The eDP application is started from the analyze tab in the Infiniium GUI. When selected and finished loading, the screen in Figure 1 is presented. This screen looks much like other applications in the Infiniium framework. Of particular note, after selecting the standard to test (eDP) and the test suite (High-Speed Physical Layer Tests) are the Device Definition and Test Setup buttons.

These are selected in progression, Device Definition first and then Test Setup. You can test with the device definition defaults (determined by the template the user can set) and with the connections defined without any further manipulations. You can proceed to Select Tests tab to select tests you want to run for the test session and continue to running tests.

Embedded DisplayPort Test Application eDP Device 1	
<u>F</u> ile <u>V</u> iew <u>T</u> ools <u>H</u> elp	
Set Up Select Tests Configure Connect Run Automate Results	HTML Report -
Embedded DisplayPort Test App	lication Test Environment Setup
Test Specification	Test Selection
eDP 1.4b	Physical Layer Tests
Test Environment Setup	
Device Definition Setup Test Setup	
Device Definition Setup Completed. Test Setup Incomplete	
Show Normative Tests Only	
Test Controller Setup	
Test Controller UnigrafDPTC 🔽 🗌 Enable Automation Configur	e
Script File C:\Program Files\Keysight\Infiniiur Browse Test Co	ntroller Dialog
Messages	•
Summaries (click for details)	Details
2019-10-11 04:22:31:331 PM Refreshing HTML Report	Application initialized and ready for use.
2019-10-11 04:22:31:414 PM HTML Report Refreshed	
2019-10-11 04:22:31:526 PM Refreshing HTML Report	
2019-10-11 04:22:31:560 PM HTML Report Refreshed	
2019-10-11 04:22:31:779 PM Connecting to The primary oscillos	
2019-10-11 04:22:32:247 PM Connected to The primary oscillosc	
2019-10-11 04:22:33:608 PM Refreshing HTML Report	
2019-10-11 04:22:33:628 PM HTML Report Refreshed	
2019-10-11 04:22:33:628 PM HTML Report Refreshed 2019-10-11 04:22:49:987 PM Ready	
	•

Figure 1. eDP test environment setup.

#### **Device Definition**

The Device Definition tab is where much of the eDP EPV software's power resides. When you click on the Device Definition Setup button, you will see a sequence of windows for you to define your device's capabilities and the specifications for these. You can see in Figure 2 how much information is shown in the second tab, Link Rate.

Device Definition Wizard								
eDP Device 🛛 Link Rate 🛛 Level 🛛 Eye Diagram 🗍 Jitter 🔹 Rise/Fall Time 🗍 Inter Pair Skew 🛛 Main Link And SSC 🗍 Intra Pair S 🗨 🕨								
Link Rate								
Reference Clock Frequency: 270 - MHz								
Specification Limit Unit Type: O bps								
Number of Link Rates: 4 -								
Link Rate 1 : 1.62 🗸 Gbps 617.3 ps RBR Min: -5300 ppm Max: 300 ppm Equalizer								
Link Rate 2 : 2.7 🗸 Gbps 370.4 ps HBR Min: -5300 ppm Max: 300 ppm Equalizer								
Link Rate 3 : 5.4 🗸 Gbps 185.2 ps HBR2 Min: -5300 ppm Max: 300 ppm Equalizer								
Link Rate 4 : 8.1 🗸 Gbps 123.5 ps HBR3 Min: -5300 ppm Max: 300 ppm Equalizer								
Spread Spectrum Clocking								
Spread Spectrum Clocking State : Settable -								
SSC Modulation Frequency 32 kHz Min: 30 kHz Max: 33 kHz								
SSC Modulation Deviation -2500 ppm Min: -5000 ppm Max: 0 ppm								
<< Back Next >> Close								

Figure 2. Link rate tab in Device Definition sequence

First, note that the tabs across the top of the window cover not only the device capabilities such as link rate and level but also capture the details necessary for all the tests that can be conducted. (Example: For eye diagram testing, you can set the pattern at which to test as well as the mask file to be used.)

The fundamental issues for eDP testing are addressed with this screen, and they are:

- The number of bit rates of which the device is capable.
- The nominal values of those bit rates.
- The manner to display the frequency accuracy of those bit rates: absolute error (bps) or ppm versus nominal link rate value. The minimum and maximum values are displayed for convenience.
- The CTLE (continuous time linear equalizer) attributes you want to use in the analysis measurements (eye diagram and jitter) to use for each bit rate.

These are defaulted to the values recommended in the VESA **eDP standard** but are easily alterable. Finally, since spread spectrum clocking (SSC) is a favored technique in embedded systems to keep EMI low, the SSC tests parameters and specifications are selectable here. It can be set to 'Always On,' 'Always Off,' and 'Settable.' When the entries for the Link Rate window are complete, you will press 'Next' and proceed to the Eye Diagram and Jitter tabs to complete the product and test requirements. Figure 3 shows attributes of the Jitter tab and, at the same time, illustrates a very useful construct called Test Plan.'

Embedded Dis	olayPort Test A	pplicatio	on eDP Devi	ce 1							X
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	Device Definition		1					1			
Test Specificatio	eDP Device Link F	Rate   Leve	I Eye Diagram JI			Pair Skew   Maii	n Link And SSC	Intra Pair S 💶			
				Jitt						$\mathbf{\overline{\mathbf{v}}}$	
Test Environme	Link Rate	Equalizer Enabled	Test Pattern	Test Plan	Non ISI Max (UI)	TJ Max (UI)	DJ Max (UI)	RJ Max (UI)		<u>_</u>	
	Link Rate 1		HBR2CPAT -	Edit	276.0 m	500.0 m	410.0 m	230.0 m			
တ Device De		•	HBR2CPAT -	Edit	276.0 m	500.0 m	410.0 m	230.0 m	_		
Device Definitio			HBR2CPAT -	Edit	276.0 m	500.0 m	410.0 m	230.0 m			
🧧 🗹 Show Norm	Link Rate 4	~	HBR2CPAT 👤	Edit	276.0 m	600.0 m	410.0 m	100.0 m			
Test Controller	Test Plan Wizard										
Test Controller		TestP	lan								
Script File C:\F Messages Summaries (clic 2019-10-11 04 2019-10-11 04 2019-10-11 04 2019-10-11 04 2019-10-11 04 2019-10-11 04 2019-10-11 04	Different	e late4 (8.1 G ial Voltage L evel0 (200 r evel0 (250 r evel3 (350 r hasis Level reEmphasis reEmphasis reEmphasis l Refresh	bps) .evel nV) nV) nV) nV) 0 (0.000dB) 1 (2.000dB) 2 (4.000dB) 2 (4.000dB) Cance	osci	3_EQ << Bac llosc	:k N	ext >>	Close	ıse.		~
Unsaved Change	s 0 Tests										

Figure 3. Jitter setup in the device definition sequence

In the Jitter Setup window, you will immediately see how comprehensive and flexible the software is. Firstly, it allows for all the link rates to be tested for jitter and allows for pattern type selection for the jitter measurement (selections are: PRBS7, HBR2CPAT, D10.2, random pattern). Then, you can enter the upper limits of jitter in the various components of jitter. Since the capability of your device includes different level settings and pre-emphasis settings, you might be interested in testing jitter for ALL combinations of these or just a few. By simply clicking the boxes in the Test Plan Wizard, you can select the device combinations to be tested.

When you have finished with the Jitter setup, you can save the setup as a template for the next time you test. Further, you can send this template to a colleague or partner so they can use the same setup, conditions and test line limits. You will see a status label below the Device Definition button, and you can click on this to select another template. At this time you now click the Test Setup button and Connection Setup button to enter the Test Session details: attributes of your work bench and test connection.

🗹 Embedded DisplayPort Test Application eDP Device 1
<u>F</u> ile <u>V</u> iew <u>T</u> ools <u>H</u> elp
Set Up Select Tests Configure Connect Run Automate Results HTML Report
Embedded DisplayPort Test Application Test Environment Setup Test Specification  eDP 1.4b  Test Setup  Test Environment Setup  Device Definition Setup Device Definition Setup Completed. Test Setup Connection Setup Completed. Test Setup Connection Setup Completed. Show Normative Tests Only  Test Controller Setup Test Controller Setup Script File C:\Program Files\Keysight\Infinitur Browse Test Controller Dialog
Messages
Summaries (click for details) Details
2019-10-11 04:22:31:414 PM HTML Report Refreshed 2019-10-11 04:22:31:526 PM Refreshing HTML Report 2019-10-11 04:22:31:560 PM HTML Report Refreshed 2019-10-11 04:22:31:779 PM Connecting to The primary oscillos 2019-10-11 04:22:32:247 PM Connected to The primary oscillos 2019-10-11 04:22:33:608 PM Refreshing HTML Report 2019-10-11 04:22:33:608 PM Refreshing HTML Report 2019-10-11 04:22:33:628 PM HTML Report Refreshed 2019-10-11 04:22:33:628 PM HTML Report Refreshed 2019-10-11 04:22:39:79 PM Ready 2019-10-11 04:22:39:79 PM Ready 2019-10-11 04:22:39:79 PM Ready 2019-10-11 04:22:30:70 PM Ready 2019-10-11 04:22:30 PM Ready 2019-10-11 04:20 PM Ready 2019-10-10 PM Ready 2019-10-10 PM Ready 2019-10-10 PM Ready 2019-10 PM Ready 2019-10 PM Ready

Figure 4. When finished with device setup, your specific template file is loaded.

## **Test Session**

The eDP EPV test session wizard is leveraged from the DisplayPort test software wizard. Its purpose is to identify the connection to the oscilloscope and enable selecting the scope of testing for your current test session – say because of troubleshooting. For example, though a device might be defined in the Device Definition wizard, to have 4 bit rates and 4 lanes, you might be interested in only one lane and the eye diagram of one bit rate for a given experiment or characterization. The session test sequence is four screens, the purpose of which is to specify connection to the oscilloscope and to select only what you need for your immediate test objectives.

## **Test Setup**

The Test Setup dialog allows you to narrow in on a specific lane, bit rate or level for a focused characterization test. The screen is shown below:

Test Setup			? 🗆 🗙
_ID		Comments –	]
Device ID			
Operator ID			
Project ID			
DUT Info		Test Info —	]
Device Type Source		Test Type	Differential Tests 🛛 💟
DUT Definition			
Lane Setting —	Bit Rate ——		Spread Spectrum Clocking
📄 1 Lane	🗹 Bit	Rate 1	🖌 SSC Disabled
🔵 2 Lanes	🗹 Bit	Rate 2	🖌 SSC Enabled
4 Lanes	🖌 Bit	Rate 3	
	🚽 🖌 🖌 Bit	Rate 4	
Voltage Level	Pre-Emphasis	Level ———	Post-Cursor 2 Level
🖌 Swing 0	🗹 Pre-ei	mphasis 0	🖌 Level 0
🖌 Swing 1	🗹 Pre-ei	mphasis 1	
🖌 Swing 2	🖌 Pre-ei	mphasis 2	
Swing 3	📝 Pre-ei	mphasis 3	
			OK Close

Figure 5. eDP session test details in setup.

You can select the specifics to test easily. For instance, if you just want to test 5.4 Gbs (bit rate 4), you would choose bit rate 4 and leave the other bit rates unselected. If you select all the bit rates for all the tests you selected in the test select tab, the software will run at all the bit rates you have selected.

## **Connection Setup**

The Connection Setup dialog is the channel assignment setup. It will portray the connection expected in number of channels and type of connection requested. It is editable, and if there are channel assignment conflicts, the user is alerted to the fact. In a prior screen, you can select whether you want to use direct connection to the oscilloscope or connect with oscilloscope differential probes. Direct connection is recommended; however, using differential probe heads (SMA probe heads), you can connect four lanes simultaneously and measure all the differential tests in one test connection

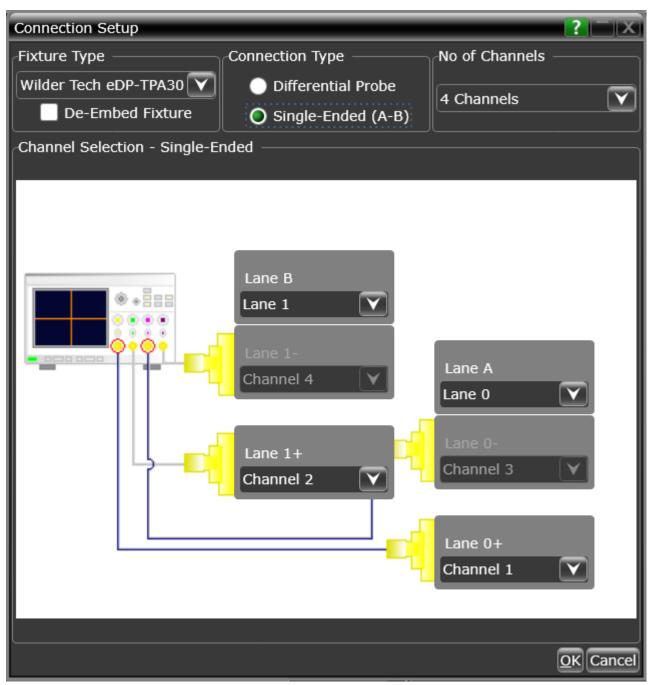


Figure 6. Channel assignment setup: lane and oscilloscope assignment: 2 lane single-ended connection using all four scope channels.

#### **Test Selection**

After defining the test environment through the Test Setup and Connection Setup, you are presented with only those tests that are appropriate for the device defined AND environment chosen. For example, if spread spectrum clocking (SSC) is not selected in the session description, then no SSC tests will appear; nor will they regardless of if the device definition setup defined the device to be SSC OFF only. A similar logic holds for pre-emphasis and levels as well. If your device definition is one lane only or defined device connection is one lane (one differential probe or two single-ended connections), then no inter-pair skew

tests will appear in the test suite. This dynamic filtering simplifies your job by ensuring you attempt to test only what is possible for the DUT and connection model you have chosen.

The eDP test suite is shown in the test selection screen (see Figure 7). It is partitioned in groups of tests as a function of the pattern that is required to test. By grouping them so, the number of required test interruptions is minimized. Shown is D10.2 (clock pattern), PRBS7 (127-bit repetitive pattern), and HBR2CPAT, which is a 2520-bit repeating pattern that was defined specifically for HBR2 in DisplayPort 1.2 – it is considered a key pattern to test with in most circumstances. Other patterns that may be used are PLTPAT (divide-by-10 clock) and random pattern, which is offered for flexibility.

Tests may be selected independently, and any number of tests may be selected for a given run. If more than one lane is possible to run (as determined by the selections in setup), then test selection by lane is also possible. If different connections or conditions of test are required from one test to another, a splash screen is presented to the user indicating the required change.

Embedded DisplayPort Test Application eDP Device 1	
<u>File V</u> iew <u>T</u> ools <u>H</u> elp	
Set Up Select Tests Configure Connect Run Automate Results	HTML Report
Embedded DisplayPort Tests	
Source Tests	
Source Differential Tests	
HBR2CPAT Tests	
▹ ✓ Eye Diagram (TP3_EQ)	
<ul> <li>Non ISI Jitter</li> </ul>	
<ul> <li>Total Jitter (TP3_EQ)</li> </ul>	
رم > Deterministic Jitter (TP3_EQ)	
Random Jitter (TP3_EQ)	
PRBS 7 Tests	
Peak to Peak Differential Voltage	
Differential Voltage Level	
Pre-Emphasis Level	
ဟ ၊ Inter Pair Skew	
D10.2 Tests	
Main Link Frequency Compliance	
SSC Modulation Frequency	
SSC Modulation Deviation	
PLTPAT Tests     Differential Transition Time	
, Differential transition time	
(Click a test's name to see its description)	^
Messages	•
Summaries (click for details)	Details
0 2019-10-11 04:22:31:414 PM HTML Report Refreshed	You have selected to close the device definition wizard, your
2019-10-11 04:22:31:526 PM Refreshing HTML Report	device definition setting will not be saved to defined file.
2019-10-11 04·22·31·560 PM HTML Report Refreshed	[No] and continue on wizard setting
Unsaved Changes 6 Tests	

Figure 7. Lists the tests that are selectable and their status. Status bubbles indicate successful completion, failure or incompletion

#### Configurability and Guided Connection

The eDP Electrical Performance Validation software provides further flexibility in your test setup through the configure tab and will guide you to make connection changes with hookup diagrams when the tests you select require it.

While the most configurability is afforded in the test definition sequence, the configure tab allows for further possibility of modification of the test session operation for testing debug or 'what-if' analysis. For instance, you can alter transfer function, equalization or bandwidth of the measurement. In Figure 8, you can see some of the configurable parameters that can be altered in a given test session.

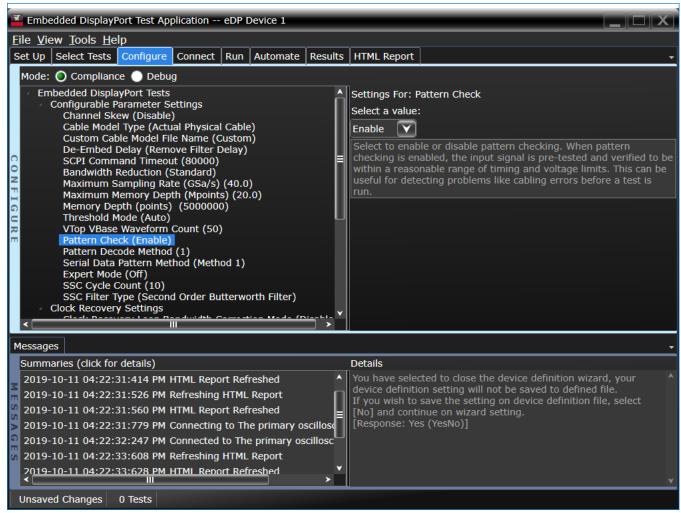


Figure 8. The eDP configure tab enables changing measurement parameters in the 'Debug' mode to support characterization and debug activities.

After you configure the test to meet your needs, the eDP EPV user interface displays the connection screen, which is specific to the configuration data you have selected. Figure 9 illustrates the typical connection guidance provided for a two-channel 'A minus B' connection model for a two lane test setup.

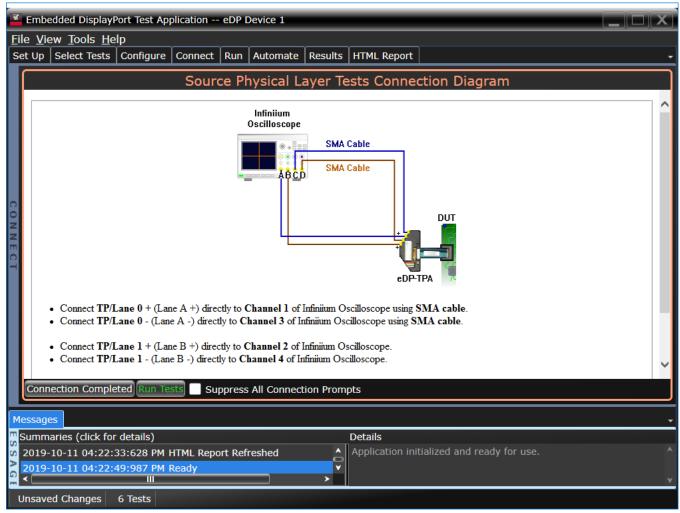


Figure 9. The final step before test is to illustrate the anticipated connection for the test.

Embedded Display	Port Test Application eDP Device 1			
File View Tools He				
	Configure Connect Run Automate	Results HTML	Report	•
Test Name		Actual Value	Margin %	Pass Limits
🗸 Lane 0 - Eye Diag	ram Test (TP3_EQ) (HBR2CPAT)	0.000	50.0	-500 m <= VALUE <= 500 m
🥑 Lane 0 - Non ISI	Jitter Test (HBR2CPAT)	94.3000 mUI	65.8 <sup>v</sup>	VALUE <= NonISIJitterLimit UI
Lane 0 - Total Jitt	er Test (TP3_EQ) (HBR2CPAT)	431.500 mUI	28.1	VALUE <= TotalJitterLimit UI
Lane 0 - Determi	nistic Jitter Test (TP3_EQ) (HBR2CPAT)	375.000 mUI	8.5	VALUE <= DeterministicJitterLimit UI
Lane 0 - Random	Jitter Test (TP3_EQ) (HBR2CPAT)	5.400 mUI	94.6	VALUE <= RandomJitterLimit UI
		-1.689830 kppm		MainLinkFrequencyPPMMinLimit ppm <= VALUE <
	Julation Frequency Test (D10.2)			SSCModulationFrequencyMinLimit Hz <= VALUE <
~	Julation Deviation Test (D10.2)	-3.784398 kppm		SSCModulationDeviationMinLimit ppm <= VALUE
📅 🚽 Lane 0 - Rise Tim ဖ <	e Test (PLTPAT) III	151.338 ps	7.9	RiseTimeMinLimit s <= VALUE <= RiseTimeMaxLir *
Trial Summary Completed: 15 Passed: 15 Failed: 0 Worst: 1 Max Displayed: 30	Mean         0.000         50.000 %           StdDev         0.000         0.000 %           Range         0.000         0.000 %           Min         0.000         50.000 %           Max         0.000         50.000 %           Sum         0.000         750.000 %           Trial 1         0.000         50.0%         1.0           Trial 2         0.000         50.0%         1.0           Trial 3         0.000         50.0%         1.0           Trial 4         0.000         50.0%         1.0           Trial 5         0.000         50.0%         1.0	0000000 M 0000000 M 0000000 M 0000000 M 0000000 M 0000000 M Eye N Eye N	meter ditional Inf ber of UI width Height (VI Height (VI Width Meas Height Meas Height Meas	High) Low) sured
Messages Summaries (click for 2019-10-11 04:22: 2019-10-11 04:26: < 13 Tests	,	Details		▼ lized and ready for use.

Figure 10. eDP EPV test software results report documents your test and indicates the pass/ fail status, test specification range, measured values and margin.

#### **Thorough Performance Reporting**

The eDP Electrical Performance Validation software generates thorough reports that not only capture the performance and status of the device under test, but also capture the screen shots of your most significant measurements for your perusal and evaluation. The first page of the report lists equipment and configuration details required in standard quality-assurance programs. It also provides a hot-linked results table that will quickly get you to the measurement report section of interest.

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		Name		Applica 9040EDPV eDP			
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				DP 1.4b hysical Layer Tes	to		
				InigrafDPTC			
		Fixtu	е Туре	Vilder Tech eDP-1	PA30		
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Failed Passed Total largin Th Warnin Critica	stics         0           13         13           13         13           13         13           13         13           13         13           13         13           13         13           13         13           13         13           13         13           14         15           15         15           15         15           15         15           15         15	S Test Name Lane 0 Eye Diagram Test (TP3 EQ) (HBR2CPAT) Lane 0 Mon ISI Jiffer Test (TP3 EQ) (HBR2CPAT) Lane 0 Total Jiffer Test (TP3 EQ) (HBR2CPAT) Lane 0 Deterministic Jiffer Test (TP3 EQ) (HBR2CPAT) Lane 0 Main Jiffer Test (TP3 EQ) (HBR2CPAT) Lane 0 Main Link Frequency Compliance Test (D10 2)	0.000 94.3000 mUI 431.500 mUI 375.000 mUI 5.400 mUI -1.689830 kp	50.0 % 65.8 % 28.1 % 8.5 % 94.6 % 35.5 %	S00 m <= VALUE <= 500 m VALUE <= NonISUlterLimit UI VALUE <= TotaJitterLimit UI VALUE <= DeterministiGitterLimit UI VALUE <= RandomJitterLimit UI MainLinkFrequencyPPMMinLimit ppm <= VALUE <= MainLinkFrequencyPPMMaxLimit		
Failed Passed Total Margin Th Warnin Critica	stics 0 13 13 13 13 13 13 15 15 15 15 15 15 15 15 15	Test Name Lane 0 - Eve Diagram Test (TP3 EQ) (HBR2CPAT) Lane 0 - Non ISI Jitter Test (HBR2CPAT) Lane 0 - Determinical Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 - Determinical Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 - Random Jitter Test (TP3 EQ) (HBR2CPAT)	0.000 94.3000 mUI 431.500 mUI 375.000 mUI 5.400 mUI	50.0 % 65.8 % 28.1 % 8.5 % 94.6 % 39.9 %	S00 m <= VALUE <= 500 m VALUE <= NonISUtterLimit UI VALUE <= TotaJitterLimit UI VALUE <= DeterministicJitterLimit UI VALUE <= RandomJitterLimit UI	iit Hz	
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Failed Passed Total Margin Th Warnin Critica	stics 0 13 13 13 13 13 13 15 15 15 15 15 15 15 15 15 15	Test Name Lane 0 - Eve Diagram Test (TP3 EQ) (HBR2CPAT) Lane 0 - Non ISI Jitter Test (HBR2CPAT) Lane 0 - Non ISI Jitter Test (HBR2CPAT) Lane 0 - Total Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 - Radow Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 - Nam Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 - SSC Modulation Frequency Compliance Test (D10 2) Lane 0 - SSC Modulation Frequency Test (D10 2) Lane 0 - Rise Time Test (PLTPAT)	0.000 94.3000 mUI 431.500 mUI 5.400 mUI -1.689830 kp 31.196 kHz -3.784398 kp 151.338 ps	50.0 % 65.8 % 28.1 % 94.6 % 35.5 % 39.9 % 39.9 % 24.3 %	S00 m <= VALUE <= 500 m VALUE <= NonISUtterLimit UI VALUE <= TotaJitterLimit UI VALUE <= DeterministicJitterLimit UI VALUE <= RandomJitterLimit UI VALUE <= RandomJitterLimit UI MainLinkFrequencyPPMMaxLimit ppm <= VALUE <= MainLinkFrequencyPPMMaxLimit SSCModulationPevalandMinLimit Hz <= VALUE <= SSCModulationFrequencyMaxLimit RiseTimeMinLimit s <= VALUE <= RiseTimeMaxLimit s	iit Hz	
Failed Passed Total Margin Th Warnin Critica	Image: state	Test Name Lane 0 Eye Diagram Test (TP3 EQ) (HBR2CPAT) Lane 0 Non IS- Inter Test (HBR2CPAT) Lane 0 Total Vittler Test (TP3 EQ) (HBR2CPAT) Lane 0 Random Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 Random Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 Random Jitter Test (TP3 EQ) (HBR2CPAT) Lane 0 SSC Modulation Frequency Test (D10 2) Lane 0 SSC Modulation Persition Test (D10 2) Lane 0 SSC Modulation Persition Test (D10 2) Lane 0 Rand Time Test (PLTPAT)	0.000 94.3000 mUI 431.500 mUI 5.400 mUI -1.689830 kp 31.196 kHz -3.784398 kp 151.338 ps 149.746 ps	50.0 % 65.8 % 28.1 % 8.5 % 94.6 % 39.9 % 39.9 % 39.9 % 7.9 % 9.3 %	S00 m <= VALUE <= 500 m VALUE <= NonISUIteI_Init UI VALUE <= TotAlUIteI_Init UI VALUE <= TotAlUIteI_Init UI VALUE <= AndomiliteI_Init UI VALUE <= RandomiliteI_Init UI VALUE <= RandomiliteI_Init pm <= VALUE <= ManLinkFrequencyPPMMaxLimit SSCModulationFrequencyMnLimit pm <= VALUE <= SSCModulationPrequencyMaxLimit SSCModulationDeviationMinLimit pm <= VALUE <= SSCModulationDeviationMaxLimit ResTimeMnLimit s <= VALUE <= ResTimeMaxLimit s FallTimeMinLimit s <= VALUE <= FallTimeMaxLimit s	iit Hz	

Figure 11. The eDP software generates a summary report where you can see the total test results for your device quickly and clearly. Additional details are available for each test, including the test limits, test description and test results, including waveforms, if appropriate. All are hotlinked to more detailed results further in the report. In addition, the margin of the result is indicated to provide further insight.

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(Worst)	0.000		1.000000 M mUI	mV	-37.500 mV	86.170 ps	424.000 mV	410 mUI	0.000 V	0.000000 UI Compliance Trysical Layer Tests	Source	Both	(A-B)	4 Gbps	1 250 mV	0.000dB	Enabled	Level 0
Trial 2	0.000	50.0%	1.000000 M 400.000 mUI	37.500 mV	-37.500 mV	86.170 ps	282.000 mV	420 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 8.1 4 Gbps	Swing 200 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
Trial 3	0.000	50.0%	1.000000 M 400.000 mUI	37.500 mV	-37.500 mV	75.400 ps	254.000 mV	390 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 8.1 4 Gbps	Swing 200 mV	Pre-emphasis 2.000dB	SSC Enabled	Level 0
Trial 4	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	152.280 ps	479.000 mV	540 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 5.4 3 Gbps	Swing 250 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
Trial 5	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	139.330 ps	403.000 mV	480 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 5.4 3 Gbps	Swing 250 mV	Pre-emphasis 2.000dB	SSC Enabled	Level 0
Trial 6	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	154.330 ps	319.100 mV	410 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 5.4 3 Gbps	Swing 200 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
Trial 7	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	137.890 ps	303.000 mV	470 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 5.4 3 Gbps	Swing 200 mV	Pre-emphasis 2.000dB	SSC Enabled	Level 0
Trial 8	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	344.580 ps	521.900 mV	490 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 2.7 2 Gbps	Swing 250 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
Trial 9	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	328.360 ps	463.000 mV	390 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 2.7 2 Gbps	Swing 250 mV	Pre-emphasis 2.000dB	SSC Enabled	Level 0
Trial 10	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	347.090 ps	353.500 mV	420 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 2.7 2 Gbps	Swing 200 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
Trial 11	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	328.990 ps	345.700 mV	390 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 2.7 2 Gbps	Swing 200 mV	Pre-emphasis 2.000dB 1	SSC Enabled	Level 0
Trial 12	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	574.320 ps	528.000 mV	390 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 1.62 1 Gbps	Swing 250 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
Trial 13	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	548.430 ps	492.000 mV	380 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 1.62 1 Gbps	Swing 250 mV	Pre-emphasis 2.000dB	SSC Enabled	Level 0
Trial 14	0.000	50.0%	1.000000 M 500.000 mUI	37.500 mV	-37.500 mV	570.930 ps	356.800 mV	540 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended (A-B)	Bit Rate 1.62 1 Gbps	Swing 200 mV	Pre-emphasis 0.000dB	SSC Enabled	Level 0
						551.850 ps	368.500 mV	380 mUI	0.000 V	0.000000 UI Compliance Physical Layer Tests	Source	Both	Single-Ended	Bit Rate 1.62	Swing 200 mV	Pre-emphasis 2.000dB	SSC	Level 0
Lane 0 - Eye Di PAT) ight Inf:	Iniium	B_EQ) : Tues	1.000000 M S00.000 mUI day, September	37.500 mV	-37.500 mV	331.030 ps				, iests			(A-B)	1 Glops	0 200 100	1	Enabled	
Lane 0 - Eye Di IPAT) 1ght Inf: 160 mV	lagram (TP3 1111um / -2.8 2al-Time 1.19682	3_EQ) : Tues 32 mV : Eye				551.630 ps				636 mV 477 mV 317 mV			(A-8)	1 Gibps	0	1	Enabled	
ane 0 - Eye Di PAT) 1ght Inf: 160 mV	agram (TP3 iniium / -2.8 eal-Time	3_EQ) : Tues 32 mV : Eye	day, September		32:50 FM	84 00.1CC				636 mV 477 mV			(A-8)	1 Gbps	0	1	Enabled	
ane 0 - Eye Di PAT) 1ght Inf: 160 mV	lagram (TP3 1111um / -2.8 2al-Time 1.19682	3_EQ) : Tues 32 mV : Eye	day, September		32:50 PM					636 mV 477 mV 317 mV 157 mV			(A-8)	1 Gibps	0	,	Enabled	
Lane 0 - Eye Di IPAT) 1ght Inf: 160 mV	lagram (TP3 1111um / -2.8 2al-Time 1.19682	3_EQ) : Tues 32 mV : Eye	day, September		32:50 FM					636 mV 477 mV 317 mV - 3 mV - 163 mV - 322 mV			(A-8)	1 Gibps	0	1	Enabled	
Lane 0 - Eye Di IPAT) 1ght Inf: 160 mV	lagram (TP3 1111um / -2.8 2al-Time 1.19682	3_EQ) : Tues 32 mV : Eye	day, September		32:50 FM					636 mV 477 mV 317 mV 157 mV - 3 mV - 163 mV - 322 mV - 482 mV			(4-8)	1 Gibps	0	1	Enabled	
Lane 0 - Eye Di IPAT) 1ght Inf: 160 mV	lagram (TP3 1111um / -2.8 2al-Time 1.19682	s_EQ) : Tues 32 mV : Eye MUI	day, September	24, 2019 8:	32:50 PM	223 ps	446 ps	668 ps	83.1 ps	636 mV 477 mV 317 mV - 3 mV - 163 mV - 322 mV			(4-8)	1 Gibps	0	1	Enabled	
ane 0 - Eye Di PAT) 1ght 1nf: 160 mV	egram (TP3 Enllum / -2.8 eal-Time 1.19682 5 Wfms -89.1 ps	s_EQ) : Tues 32 mV : Eye MUI	day, September ● > □	24, 2019 8:	32:50 PM				89.1 ps	636 mV 477 mV 317 mV 157 mV -3 mV -163 mV -322 mV -642 mV -642 mV			(4-8)	1 Gbps	0	,	Enabled	
Lane 0 - Eye Di IPAT) 1 160 mV	agram (TP3 11110m / -2.6 231-Time 231-Time 231-Time 235 Wfms -89.1 ps -89.1 ps 0.0 s	EQ) I Tues 32 mV Eye MUI	day, september	24, 2019 8:	32:50 PM				89.1 ps	636 mV 477 mV 317 mV 157 mV -3 mV -163 mV -322 mV -642 mV -642 mV			(4-3)	1 Obys	0	,	Enabled	
Lane 0 - Eye Di (PAT) (160 mV) (160 mV) (160 mV) (110 mV) (1	agram (TP3 / [-2.8 - 2.9 - 2.9	8_EQ) : 1ues 32 mV Eye MUI	day, september	24, 2019 8:	32:50 PM				89.1 pz	636 mV 477 mV 317 mV 157 mV -3 mV -163 mV -322 mV -642 mV -642 mV			(4-3)	1 Obys	0	, ,	Enabled	

Figure 12. Summary report detail: The eDP software's summary report provides screen shots of all the measurements that have been performed. In this figure, you can see that many data-eye measurements were made (15 trials) and the first trial screen shot is shown. Observe the clear status and description at the top and the measurement data just above the eye.

## eDP Test Point Adapters

The eDP specification is standardized on I-PEX connectors on the display panel to connect to a graphics processor board/motherboard through a ribbon-like flexible PC board.



Figure 13. I-PEX connector with ribbon-like flexible PC board.

By virtue of this standardization, testing for eDP must be done at the panel connector. In DisplayPort and eDP, this point is called Testpoint 3 (or TP3 for short). TP3 necessarily includes the loss of the ribbon cable and whatever connection characteristics are at the motherboard where the ribbon connector is connected. To acquire at TP3, you will need a mating connector to your I-PEX connectorized flexible PC board. Wilder Technologies makes a family of products to connect to the flexible PC board; these are identified in the Test Accessories table below.

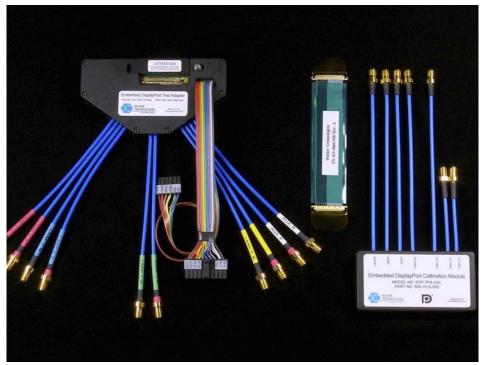


Figure 14. Wilder Technologies' eDP-TPA40L-PC test point adapter fixture.

This eDP fixture has high-speed breakout cables that terminate with SMA female connectors with an assumption that there will be cables from the oscilloscope channels to the fixture. While these cables do increase loss to the measured lines, they can be kept to a minimum to reduce their effect and can be effectively removed using PrecisionProbe software available in the Infiniium oscilloscope (see Table 4).

While TP3 will show the actual performance through a flexible PC board, it is often desired to render the acquired waveform in 'compensated' fashion to simulate a minimal correction that a receiving device might make. In DP and eDP, we call this TP3EQ (or TP3 equalized). We use CTLE (continue time linear equalizer) equalization, and the parameters for the CTLE are given in the eDP specification. The settability of these is discussed above in Device Definition.

## Extensibility

You may add additional custom tests or steps to your application using the User Defined Application (UDA) development tool (www.keysight.com/find/uda). Use UDA to develop functional "Add-Ins" that you can plug into your application.

Embedded DisplayPort Test Application	n eDP Device 1		
File View Tools Help			
Connect to Infiniium	t Run Automate Results	HTML Report	-
New Project	nbedded DisplayPort Test Appl	ication Test Environment Setup	
Open Project		Test Selection	
Save Project		Physical Layer Tests	
Save Project As			
Save Project (Settings Only) As	Test Setup		
Export Results	Test Setup Incomplete		
User Defined	Install Add-In		
Print			
Print Preview	able Automation Configure		
Page Setup	nfiniiur Browse Test Con	troller Dialog	
Exit			
Messages			-
Summaries (click for details)		Details	
0 0 2019-10-11 04:40:53:107 PM Ready	<u>^</u>	Application initialized and ready for use.	
∧ <sub>G</sub> <	×		
0 Tests			•

Figure 15. Importing a UDA add-in into a compliance application.

Add-ins may be designed as:

- Complete custom tests (with configuration variables and connection prompts)
- Any custom steps such as pre or post processing scripts, external instrument control and your own device control.

	File	Vie	ew Tools He	elp	9.3 (A		ц	that and	Me Sa .							
	Set	Up	Select Tests	Configure	Connect	Run	Automate	Results	HTML Report							
			🖌 User D 🖌 МуТ													
	Te	Test: MyTest														
		Pass Limits: No Result .imit Set: None														
			Margin Formu (Margin is not													
10			Remote Interf CommandLin			ldress	of scope> -	-c " <comn< th=""><th>nand&gt;"</th><th></th><th></th></comn<>	nand>"							
			RemoteAte Pi edTests?	roperties												
	Se	elect	edTests ' <tes< th=""><th>stId&gt;'</th><th></th><th></th><th></th><th></th><th></th><th></th><th></th></tes<>	stId>'												
0 1	Se	elect	edTests ' <tes< td=""><th>tId,testId,et</th><th>.&gt;'</th><th></th><th></th><th></th><th></th><th></th><th></th></tes<>	tId,testId,et	.>'											
0			RemoteAte M ereqIdsForTes													
			Parameters d> = -1001													
			Run-time Para rrentOptions		very											
	Fo	or me	ore informatio	on, please se	e the N54	52A Re	emote Progr	amming T	ōolkit documenta	ation (www.keys	ight.com/find/rpi).					

Figure 16. UDA add-in tests and utilities.

## Automation

You can completely automate execution of your application's tests and Add-Ins from a separate PC using the included Remote Interface feature (download free toolkit from www.keysight. com/find/scope-apps-sw). You can even create and execute automation scripts right inside the application using a convenient built-in client.

The Embedded DisplayPort Test Application eDP Device 1										
<u>F</u> ile <u>V</u> iew <u>T</u> ools <u>H</u> elp										
Set Up Select Tests Configure Connect Run Automate Results	HTML Report									
Execute commands from: 🔿 Script 🔵 Files Start Settings										
Commands # Configure SetConfig VARIABLE1 'VALUE1' Save As SetConfig VARIABLE2 'VALUE2'										
# Select Test ID SelectedTests ID,ID,										
# Run the Selected Tests Run										
AUTOMATE										
MAI										
Try a command: Command status:										
Messages	•									
	Details									
0 2019-10-11 04:40:53:107 PM Ready	Application initialized and ready for use.									
	¥									
Unsaved Changes 0 Tests										

Figure 17. Remote programming script in the automation tab.

The commands required for each task may be created using a command wizard or from "Remote Interface Hint" accessible throughout the user interface.

Using automation, you can accelerate complex testing scenarios and even automate manual tasks such as:

- Opening projects, executing tests and saving results
- Executing tests repeatedly while changing configurations
- Sending commands to external instruments
- Executing tests out of order

Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive:

- Interact with your device controller to place it into desired states or test modes before test execution
- Configure additional instruments used in your test suite such as a pattern generator and probe switch matrix.
- Export data generated by your tests and post-process it using your favorite environment, such as MATLAB, Python, LabVIEW, C, C++, Visual Basic etc.
- Sequence or repeat the tests and "Add-In" custom steps execution in any order for complete test coverage of the test plan.

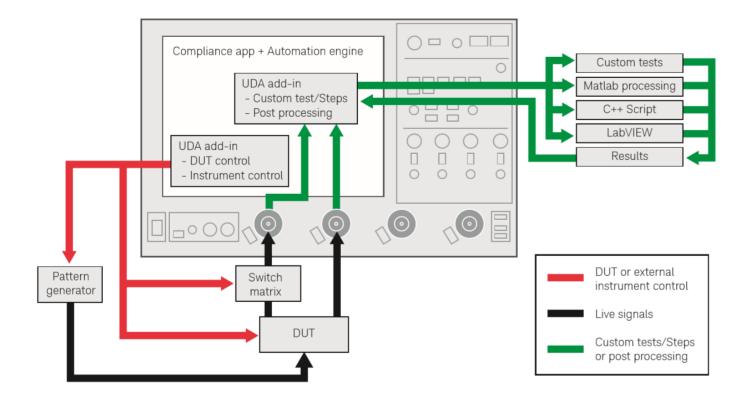


Figure 18. Combine the power of built-in automation and extensibility to transform your application into a complete test suite executive.

## **Tests Performed**

The eDP Electrical Performance Validation software performs standard tests found in the DisplayPort electrical performance and compliance software (D9040DPPC) and are provided for the specific purpose of eDP designs. Testing is assumed to be TP3 (a flexible cable from graphics processor in place) so the user needs to consider whether TP3 or TP3Eq makes sense for their application. There is nothing that prevents a Testpoint 2 measurement except test access. If a model of the flexible cable is had (S-parameter model), a transfer function can be made to undo its effects to show what the TP2 waveform looks like.

Assertion No. DisplayPort CTS 1.4b Section 3	Test Description Source Tests	Test Plan	Comments
Test ID 3.1	Data eye Diagram	Yes	Custom eye mask per data rate
Test ID 3.2	Non pre-emphasis level verification	Yes	Selectable: Referential or Absolute
Test ID 3.3	Pre-emphasis level verification	Yes	Selectable:Referential or Absolute
Test ID 3.5	Intra-pair skew	Yes	D10.2 pattern required
Test ID 3.6	Differential transition time	Yes	User entry of thresholds
Test ID 3.10	AC common mode noise	Yes	Single-ended test connection required
Test ID 3.11	Non-ISI jitter measurements	Yes	Non-equalizable jitter
Test ID 3.12	Total jitter measurements	Yes	1E-9 BER
Test ID 3.14	Main link frequency compliance	Yes	D10.2 pattern preferred
Test ID 3.15	Spread spectrum modulation frequency	Yes	D10.2 pattern preferred
Test ID 3.16	Spread spectrum modulation deviation	Yes	D10.2 pattern preferred

DP tests performed by the eDP EPV software. DisplayPort CTS1.4b referenced for test definitions

## Ordering Information

#### Recommended oscilloscope

The eDP Electrical Performance Validation software is compatible with Keysight Infiniium Series oscilloscopes with operating software revision 6.00 or higher. For oscilloscopes with earlier revisions, free upgrade software is available at www.keysight.com/find/scope-apps-sw.

Data rate	Recommended Bandwidth	Oscilloscope
Up to HBR2 (5.4 Gbs)	13GHz minimum	Infiniium V, Z and UXR series
Up to HBR3 (8.1Gbs)	16GHz recommended	Infiniium V, Z and UXR series

Note: since there is no official compliance program, the validation engineer can choose the appropriate bandwidth for system being validated.

#### Infiniium Measurement Software

Model number	Description	Note
D9040EDPV	Embedded DisplayPort Electrical Performance Validation Software	Required
D9020ASIA	Advanced Signal Integrity Software (EQ, InfiniiSim Advanced)	Optional
D9020JITA	Jitter, Vertical and Phase Noise Analysis Software	Optional: Recommended
D9010DMBA	Precision Cable Calibration	Optional: required if using switch matrix
D9020SCNA	InfiniiScan Event Identification Software	Optional
KS6810A	Data Analytics software (1 license)	Optional

#### Unattended Testing with Probes or Switch Matrix

For one connection testing with full automation in eDP either each lane is connected to a differential probe amplifier and SMA probe head, or, a switch matrix under control of the eDP Electrical Performance Validation software is used. For accuracy, direct connection to oscilloscope as always preferred, however, Keysight enables test automation through these two methods to support validation productivity.

One Connection Solution	Description	Vendor and details
Four channel Differential Connection	Amplifiers: N280xA or N700xA Probe heads: N5444A	Keysight probe solutions supported by the D9040EDPV
Switch Matrix	BIT-2100B: BIT-4000-2114-1 modules, qty=2 (4-to-1 switches) Mainframe BIT-4000-2100-1	Bitifeye Corporation, recommended integrator for Keysight solutions. Switch Matrix supported by the D9040EDPV software.

#### Recommended Test Accessories

Model number	Description	Quantity	Purpose
eDP- TPA30L-PC	Wilder Technologies 30 pin Test Point Adapter	1 (for 2 lane testing of eDP)	For physical connection to an Embedded DisplayPort device to perform test with the
eDP- TPA40L-PC	Wilder Technologies 40 pin Test Point Adapter	1 (for 4 lane testing of eDP)	D9040eDPV software, order one or more of the these Test Point Adapters.
N9398C	DC Blocking Capacitors	2 minimum / 4 recommended	Optionally used to eliminate dc bias in generator during test.
5061-5311	3.5mm f-f adapter	4 minimum / 8 recommended	Connect matched cables to break out coaxial connector of TPA
N2823A	1 m matched cable set	2 minimum	Optional: Connect scope to TPA break outs
N5448B	0.25 m matched cable set	2 minimum	Optional: Connect scope to TPA break outs

For testing eDP devices, the following solution elements are recommended for the purposes identified:

#### **AUX Channel Controller**

The Keysight D9040EDPV DisplayPort Electrical Performance Validation software now supports test automation with the an AUX channel controller if the DP test mode is supported by the device under test.

Model Number	Description	Quantity
Unigraf DPR-100	AUX channel controller requires hardware and software license from Unigraf Oy. www.unigraf.fi	1

#### Flexible Software Licensing and KeysightCare Software Support Subscriptions

Keysight offers a variety of flexible licensing options to fit your needs and budget. Choose your license term, license type, and KeysightCare software support subscription.

#### License Terms

Perpetual – Perpetual licenses can be used indefinitely.

Time-based – Time-based licenses can be used through the term of the license only (6, 12, 24, or 36 months).

#### License Types

Node-locked – License can be used on one specified instrument/computer.

**Transportable** – License can be used on one instrument/computer at a time but may be transferred to another using Keysight Software Manager (internet connection required).

**USB Portable** – License can be used on one instrument/computer at a time but may be transferred to another using a certified USB dongle (available for additional purchase with Keysight part number E8900-D10).

**Floating (single site)** – Networked instruments/computers can access a license from a server one at a time. Multiple licenses can be purchased for concurrent usage.

#### KeysightCare Software Support Subscriptions

Perpetual licenses are sold with a 12 (default), 24, 36, or 60-month software support subscription. Support subscriptions can be renewed for a fee after that.

Time-based licenses include a software support subscription through the term of the license

Selecting your license:

- **Step 1.** Choose your software product (eg. S1234567A).
- Step 2. Choose your license term: perpetual or time-based.
- **Step 3.** Choose your license type: node-locked, transportable, USB portable, or floating.
- **Step 4.** Depending on the license term, choose your support subscription duration.

KeysightCare Software Support Subscription provides peace of mind amid evolving technologies.

- Ensure your software is always current with the latest enhancements and measurement standards.
- Gain additional insight into your problems with live access to our team of technical experts.
- Stay on schedule with fast turnaround times and priority escalations when you need support.

## Learn more at: www.keysight.com

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